GEORG-AUGUST-UNIVERSITÄT
GÖTTINGEN

Fakultät für
Physik

Bachelor's Thesis

Quality Control of Modules in the ATLAS Inner Tracker

Qualitätskontrolle von Modulen im ATLAS 'Inner Tracker'

prepared by

Leander Teich

from Göttingen

at the II. Physikalischen Institut

Thesis number:	II.Physik-UniGö-BSc-2025-02
Thesis period:	9th April 2025 until 16th July 2025
First referee:	Prof. Dr. Arnulf Quadt
Second referee:	Priv. Doz. Dr. Markus Keil

Abstrakt

Diese Arbeit untersucht die Durchführbarkeit und Leistungsfähigkeit der Parallelisierung der elektrischen Qualitätssicherungstests (QS-Tests) von RD53B Modulen, mit besonderem Fokus auf die Tests im Rahmen des YARR-Software-Framework's. Erste Tests zeigten vielversprechende Ergebnisse. Anschliessende Arbeiten am Aufbau erweiterten die Kapazität für gleichzeitige Tests von zwei auf vier Module. Die Analyse umfasste verschiedene elektrische Charakterisierungstests, insbesondere die IV-Messungen, die aufgrund dedizierter Hochspannungsquellen ein erhebliches Parallelisierungspotenzial aufwiesen. Die übrigen elektrischen QC-Tests hingegen sind, aufgrund der zugrunde liegenden Softwarearchitektur sowie des Einzelinstanz-Betriebsmodells von YARR, lediglich sequentiell durchführbar. Darüber hinaus wurde eine systematische Bewertung der Parallelisierbarkeit der auf YARR basierenden Funktionstests durchgeführt, wobei die Ausführungseffizienz verschiedener Scan-Typen betrachtet wurde. Die Ergebnisse zeigten, dass bestimmte Scan-Routinen wie MHT, TUN und PFA zwar von einer parallelen Ausführung profitieren können, die erzielten Zeiteinsparungen jedoch nicht ausreichten, um eine vollständige Parallelisierung aller Module zu rechtfertigen, da dies einen synchronen Fortschritt in allen weiteren Prozessphasen vorher und nachher erfordert hätte. Diese Arbeit zeigt, dass zwar bestimmte Tests effektiv parallelisiert werden können, jedoch grundlegende Änderungen an der bestehenden Software notwendig wären, um eine vollständige Parallelisierung aller Tests - insbesondere der elektrischen Charakterisierung - zu ermöglichen.

Stichwörter: Physik, Bachelorarbeit, YARR, ITk, Atlas Experiment, Pixel Detektor

Abstract

This thesis investigates the feasibility and performance of parallelizing the electrical quality control (QC) tests of RD53B modules, with a focus on the testing within the YARR software framework. Initial tests demonstrated the potential for parallel execution, prompting subsequent upgrades that expanded the capacity for simultaneous testing from two to four modules. The analysis included various electrical characterisation tests, notably the IV measurements, which indicated a significant degree of parallelisation potential, owing to dedicated high-voltage power supplies. Conversely, the remaining electrical QC tests were determined to be inherently sequential in nature, primarily due to the software architecture and the single-instance operational model of YARR. Furthermore, a systematic evaluation of the parallelizability of YARR based functionality tests was performed, looking at the execution efficiencies of different scan types. The results revealed that while the MHT, TUN, and PFA scan routines could benefit from parallel execution, the overall time savings did not justify running all modules simultaneously, as it required synchronised progress throughout all testing stages. This work highlights that while certain tests can be effectively parallelised, major revisions to existing software would be necessary to enable parallelisation of all tests - specifically the electrical characterisations.

Keywords: Physics, Bachelor thesis, YARR, ITk, Atlas experiment, Pixel Detector

Contents

1. Introduction

The LHC's upcoming upgrade to the High-Luminosity (HL-) LHC will significantly enhance its capabilities with a planned instantaneous luminosity of $7.5 \cdot 10^{-34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ and a planned center of mass energy $\sqrt{s} = 14\,\mathrm{TeV}$ [1]. This promises increased statistical precision and more frequent observation of rare phenomena at even higher energies than before, possibly opening the door to newly discovered physics. The upgrade however also poses significant challenges for the experiments and detectors such as ATLAS due to the ever increased data rate and radiation exposure among others. To mitigate this, the ATLAS inner detector is being replaced by an all-silicon Inner Tracker (ITk), designed to withstand the increased radiation levels and data rates for the upcoming run. The sensor modules at the heart of the upgrade are crucial to the continued operation of the ATLAS detector which is why they have to be characterised and tested meticulously beforehand and stringent standards for quality control be set in place as to prevent premature sensor failures as the hardware can not be replaced during operation [2].

This thesis will focus on precisely these quality control tests at an attempt to automate these processes in order to adequately process the ≈ 1800 modules assigned to the German ITk-Pixel cluster for testing [3]. The feasibility and degree of parallelisation of these quality control tests is to be assessed as part of an overall effort to streamline and optimize the quality control process for a higher throughput.

2. The Standard Model of Particle Physics

The Standard Model of particle physics (hereafter: SM) represents the most comprehensive theoretical framework for elucidating the fundamental principles that govern the universe, and by extension, life itself. This model offers a detailed account of the elementary particles that constitute matter and the forces through which they interact, with the notable exception of gravity among others. The SM is not only a cornerstone of contemporary physics but also a testament to humanity's enduring quest to comprehend the deepest workings of nature. The Standard Model categorises particles into two primary classes: bosons and fermions, distinguished by their intrinsic spin and represented in Figure 2.1 [4].

2.1. Bosons

Bosons are force-carrying particles characterised by an integer spin ($S = 0$ or $S = 1$). These particles mediate the fundamental forces that govern interactions between matter particles [4]. The SM encompasses three types of gauge bosons and one scalar boson, each associated with a specific quantum field theory:

- **Photon (γ)**: The mediator of the electromagnetic force, responsible for electromagnetic interactions, commonly observed in phenomena such as chemical bonding and light emission. This force acts between charged particles, with photons being charge-neutral. It is described by Quantum Electrodynamics (QED).
- **W and Z Bosons ($W^{\pm}$, Z)**: Mediators of the weak nuclear force, crucial in processes such as radioactive decay and matter-antimatter asymmetry. They are described by Quantum Flavourdynamics (QFD) [6].
- **Gluon (g)**: The mediator of the strong nuclear force, binding quarks within protons and neutrons through a threefold colour charge. It is described by Quantum

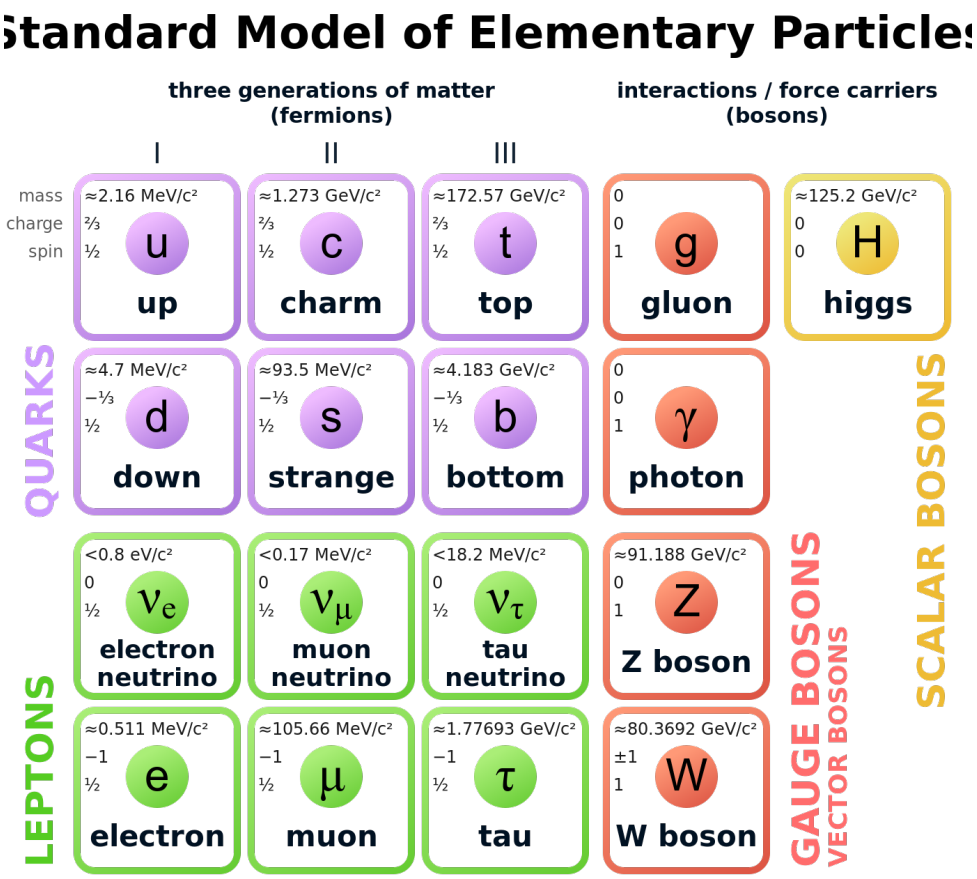

Figure 2.1.: Illustration of the known particles comprising the Standard Model. Illustration from [5].

Chromodynamics (QCD) and explains phenomena such as confinement, whereby single quarks cannot be observed independently, necessitating a bound state of at least two quarks [7–9].

- **Higgs Boson (H)**: An excitation in the Higgs field. The corresponding Higgs mechanism, which endows elementary particles with mass through their interaction with the Higgs field (H), is a crucial component of the SM, providing masses to the W and Z bosons as recently discovered by CMS and ATLAS [10, 11].

2.2. Fermions

Fermions are matter particles characterised by a half-integer spin ($S = \frac{1}{2}$). They include leptons and quarks, which can be further subdivided into three generations. The SM comprises six types of quarks, organised into three generations. Each generation consists

of an up-type quark with a charge of $+\frac{2}{3}$ and a down-type quark with a charge of $-\frac{1}{3}$ [4]. The mass of quarks increases progressively across generations [12]. Bound states of quarks (hadrons) can be further classified based on the total spin of the bound state, with baryons having a half-integer spin and mesons having an integer spin.

Similarly, the six leptons are divided into three generations, each comprising a charged particle and its neutral neutrino counterpart. Charged leptons carry a weak isospin of $-\frac{1}{2}$, while their neutral counterparts (neutrinos) have a weak isospin of $\frac{1}{2}$. The masses of charged leptons increase with each generation, whereas neutrinos, once considered massless, are now understood to possess very small but non-zero masses [12].

The intricate mathematical formalism underlying the description of interaction processes involving two or more of the aforementioned particles can be represented visually using Feynman diagrams. These diagrams serve as a shorthand for calculating the matrix elements that determine the probability amplitudes of particle interactions. Ultimately, these theoretical predictions can be implemented in Monte Carlo simulations and compared with experimentally measured cross sections to test the validity of the Standard Model and similar models.

3. Detectors

Detectors are at the heart of every high energy particle physics experiment. They are what physicists see the interesting microcosm of fundamental interactions through. Generally a detector is used to track and or identify specific particles within a collision experiment. Hereby only being able to detect the collision products, out of which the actual collision partners can be reconstructed. The sheer variety of particles and observables requires a set of different detector types with varying goals and measurement paradigms.

3.1. The LHC

Testing the predictions of the SM and peering deeper into the fundamental principles of the universe than ever before, the Large Hadron Collider (LHC) allows for groundbreaking discoveries at energies never seen before. Located at CERN (the European Centre for Nuclear Research) near Geneva, Switzerland, the LHC is an approximately 26.7 km circumference circular particle accelerator colliding beams of protons and heavy ions at a centre of mass energy up to $\sqrt{s} = 14\,\text{TeV}$ [13, 14]. A multitude of experiments are set up around these collision points including ATLAS, CMS, LHCb and ALICE, the focus of this project being the ATLAS Detector.

3.2. The ATLAS Experiment

The ATLAS (A Toroidal LHC ApparatuS) detector is one of the experiments set up at the LHC to research elementary particles and their interactions as to further our understanding of the universe, such as was the case in July 2012 when it, along with the CMS collaboration, claimed the discovery of the Higgs boson [10, 11]. It is constructed in a discrete layered, onion like fashion with different detector shells responsible for identifying different key aspects of the collision products, as illustrated in Figure 4.1 making it a general purpose detector [15]. The Inner Detector with unique tracking capabilities is followed by an electromagnetic and a hadronic calorimeter to determine energy scales as well as a final outermost muon detector to measure their respective energies.

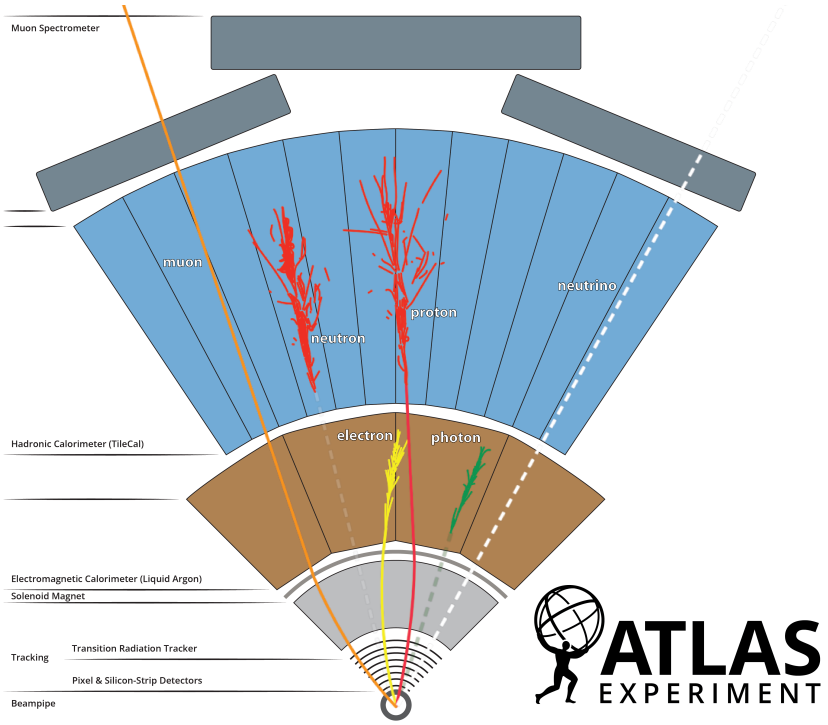

Figure 3.1.: Schematic cross-section of the ATLAS detector, illustrating its layered structure and typical penetration depths of different particles. Image by the ATLAS Collaboration [16].

Most notable and eponymous are the magnets built into the detector setup. The Atlas detector utilizes two distinct magnets to alter the path of charged collision products in order to calculate the respective energies. One being a Solenoid magnet surrounding the inner detector core reaching field strengths of up to 2 T causing trajectories of charged particles to bend in the cross sectional plane, orthogonally to the particle beam [17]. The outer most magnet being composed of a central barrel toroid and two end cap toroids provide a field strength of up to 3.9 T allowing for measurement of momenta of muons [17]. The magnet system is illustrated in Figure 3.2.

3.3. The Bethe-Bloch Formula

The Bethe-Bloch Formula (sometimes also referred to as just the Bethe Formula) describes the mean energy loss per distance travelled of a specified charged particle in the presence of matter [19, 20]. The formula and its associated functional dependencies are of significant interest in the field of particle physics, as the detectors commonly used in such experiments rely on the precise measurement of energy loss to identify and characterise particles.

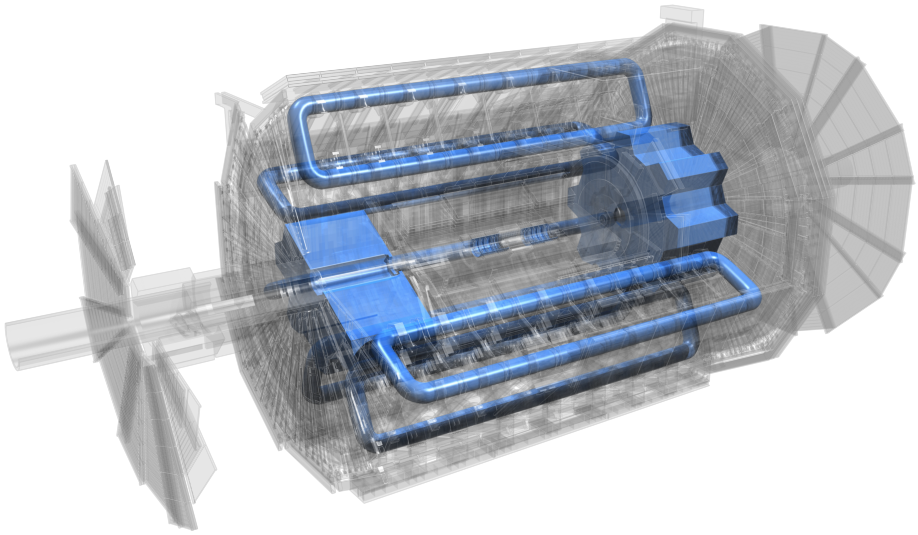

Figure 3.2.: Schematic outline of the two main magnet systems embedded into the detector. Image by the ATLAS Collaboration [18].

$$\left\langle -\frac{dE}{dx} \right\rangle = \frac{4\pi}{m_e c^2} \cdot \frac{z^2}{\beta^2} \cdot \left(\frac{e^2}{4\pi\varepsilon_0} \right)^2 \cdot n \cdot \left[\ln \frac{2m_e c^2 \beta^2 \gamma^2}{I} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right] \tag{3.1}$$

The formula 3.1 accounts for various factors, including the charge z (in units of the elementary charge) and velocity β (in units of the speed of light) of the particle, the electron density of the material $n = \frac{N_A \cdot Z \cdot \rho}{M_m \cdot A}$ (taking into account the atomic number Z, mass number A, the molar mass M_m and density ρ), and the mean excitation potential I (in eV), which collectively influence the rate of energy loss. Different parts of the curve can be attributed to different phenomena causing the energy loss, including but not limited to bremsstrahlung and ionisation. For high energies (above $\approx 10\,\text{MeV}$) the energy-loss can predominantly be attributed to bremsstrahlung and resulting e^+ e^- pair production of photons.

The radiation length is a crucial parameter in the study of electromagnetic interactions in matter, particularly in high-energy physics experiments like those conducted at the LHC. It represents the mean distance over which a high-energy electron loses all but $\frac{1}{e}$ of its energy with Euler's constant $e \approx 2.72$. Thus this characteristic length imposes boundaries on the minimum size of a given calorimeter. Bremsstrahlung and ionisation are the primary mechanisms of energy loss for charged particles traversing matter. While ionisation dominates at lower energies, bremsstrahlung becomes significant at higher energies, especially for electrons and positrons. The critical energy, E_c, is the energy at which the energy loss due to bremsstrahlung equals that due to ionisation. This energy is material-dependent and is a key factor in the design and operation of detectors.

In the context of the ATLAS detector at the LHC, understanding these processes is essential for accurate particle identification and energy measurement. The ATLAS detector uses a combination of calorimeters and tracking systems to measure the energy and momentum of particles. The calorimeters are designed to absorb and measure the energy of particles, relying on the principles of bremsstrahlung and ionisation to do so. The radiation length is particularly relevant in the design of electromagnetic calorimeters, which are optimised to measure the energy of electrons and photons by exploiting these energy loss mechanisms.

3.4. Gaseous detectors

Gaseous detectors rely on passing particles ionizing the gas within the detector volume. Through a voltage applied between the cathode and anode, the resulting electric field causes the ionised gas atoms and electrons to drift towards the respective electrode where they can be detected as an electrical signal. Depending on the voltage between the electrodes the detector can operate in different modes with a higher voltage leading to increased ionisation and thus amplifying the signals through a larger gas-amplification factor however also increasing the dead time of the detector in the process [21].

3.5. Semiconductor detectors

Semiconductor based detectors such as found in the Inner tracker of the Atlas Experiment allow for high precision trajectory reconstruction thus allowing more precise measurements of the subatomic world. The following thesis project will be mostly concerned with precisely this type of detector.

An electron within a single atom can occupy discrete energy levels as well described by quantum mechanics. When considering the energy of two or more overlapping atomic orbitals, these discrete energy levels can reshape, split and slightly shift. As a consequence of a periodic crystalline structures, the formation of high energy-level-density bands can be observed. These near to continuous regions of closely packed energy levels are referred to as an energy band. A band gap in this case refers to the absence of such regions, indicating no electrons with that energy within the observed crystal structure [22]. Generally a band can be classified as a conduction or a valence band depending on whether it lies above or below the Fermi energy, respectively. The electrical conductivity of a material is strictly dependent on the electrons in the conduction band and thus by extension also the ability of the electrons to be lifted from the valence band into the conduction band by means of

excitation (such as thermal excitation).

Materials with a partially filled conduction band (the Fermi energy lies within the conduction band) are known as conductors or metals. If the valence and conduction band are separated by a bandgap (the Fermi energy lies within the bandgap) the electrical characteristics are that of an insulator or semiconductor, depending on the energy of the bandgap. For bandgaps above $\approx 5\,\text{eV}$ materials are typically categorised as insulators due to the high energy required to excite the electrons from the valence band into the conduction band and thus allow for electrical conductivity [22]. Semiconductors are characterised by lower energy bandgaps, leading to a conductivity dependent on the energy of the electrons in the material and thus susceptible to external thermal excitation or even photoabsorption. Silicon is a common choice of semiconductor and also used in the ATLAS detector.

To further alter the electrical characteristics of a semiconductor, it can be doped. This refers to the process of introducing impurities into the crystal lattice by means of accelerating ions of other materials into the semiconductor [22]. Through a well controled heating and cooling cycle, movement at the atomic scale is introduced, allowing for the lattice structure to re-order itself and thus incorporate the doped ions. This process is known as annealing.

Generally two types of doping can be differentiated, n-Type and p-Type based on the number of valence electrons of the dopant.

- **n-type**: The dopants have more valence electrons than the base semiconductor. This leads to an excess of negative charges in the doped area.
- **p-type**: The dopants have fewer valence electrons than the base semiconductor. These electron holes result in an effective positive charge region.

Joining both p-type and n-type doped semiconductors gives rise to a fundamental building block of modern electronics, an n-p junction. Its working principle is rooted in the interaction between the two regions when they are brought into contact. At the interface of the n-type and p-type materials, electrons from the n-type region diffuse into the p-type region and recombine with holes. Equivalently, holes from the p-type region diffuse into the n-type region and recombine with electrons. This movement of charge carriers results in the formation of a depletion region, a zone around the contact area where there are no free charge carriers. The depletion region acts as an insulating barrier preventing further movement of charge carriers.

As electrons and holes recombine, they leave behind charged ions (positive ions in the n-type region and negative ions in the p-type region). This separation of charges creates

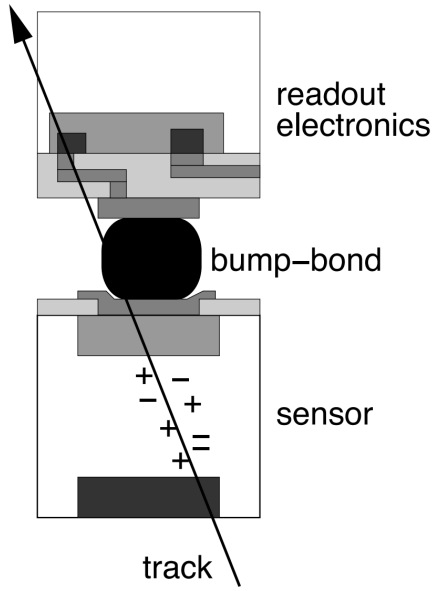

Figure 3.3.: Schematic of a single-pixel semiconductor based detector. The electron & hole pairs will, similar to as mentioned in the gaseous detectors, cause a signal in the electrode near the bump-bond through the drifting charges. Used from [23].

an electric field across the depletion region. The built-in electric field opposes further diffusion of charge carriers, establishing an equilibrium. When an external voltage is applied such that the p-type is connected to the positive terminal and the n-type to the negative terminal, the potential barrier of the depletion region is reduced. This allows charge carriers to flow across the junction, resulting in current flow. Electrons move from the n-type to the p-type region, and holes move in the opposite direction, allowing the device to conduct electricity. This is known as the forward Bias. When applying the voltage in the opposite polarity, the depletion region increases in size, even further preventing current flow across the junction. This is known as the reverse Bias [22]. Semiconductor Detectors are comprised of many individual pixels, each being an n-p junction. A passing high energy particle can excite several valence electrons inside the detector material (see 3.3) and thus create an electron-hole pair. Through the electric field across the junction, both start drifting towards opposite ends of the junction, inducing a current in the readout electronics and thus a measurable signal as illustrated in Figure 3.3.

A passing particle may also interact not by ionisation but by non-ionizing energy loss (NIEL) processes, imparting energy into the lattice structure in the form of phonons. With enough energy this can cause permanent atomic dislocation from the regular crystal structure and potentially even the removal of individual atoms from the material, introducing defects into the structure and altering the dopant concentration completely changing electrical characteristics [24]. This radiation based damage is especially detrimental to the ATLAS Inner Tracker system due to its highly intricate and microscopic

feature design as well as the spatial proximity to the beam pipe and thus large amounts of radiation.

3.6. Tracking & Vertexing

Given the data gathered by aforementioned detector types, two key techniques to further process and more easily apply to the underlying particle collision experiment are particle tracking and vertexing. Tracking is the process of determining the path taken by a detected particle as it passes through the detector system. In the presence of a magnetic field, the momentum of such charged particles can be determined, further aiding in the identification of collision products [21]. In gaseous detectors, such as drift chambers and any variation of such detector, charged particles ionize the surrounding gas, creating an ion - electron trail. Such a trail can subsequently be picked up by the nearest electrodes allowing for the measurement of a spatially resolved trajectory. Using the constant drift velocity of a particle, a trajectory can even be fully reconstructed based on the temporal segmentation of the signal such as in a time projection chamber. Semiconductor detectors have an inherently high spatial resolution, allowing for multiple layers of detectors to precisely track individual particles. Vertexing is the process of identifying the position in space where a given particle originates from, namely to reconstruct the last interaction vertex [21]. This is particularly important for studying short-lived particles which do not make it to a detector within their respective decay-length and reconstructing intermediate particle processes.

3.7. Calorimeters

Calorimeters are devices used to measure the energy of passing particles, making up the outer thicker layers of the ATLAS detector [15]. They operate on the principle of absorbing the entire energy of a particle and converting it into a measurable signal, typically through a cascade of interactions. When a high-energy particle enters the calorimeter, it undergoes a series of interactions, such as ionisation and bremsstrahlung, leading to the production of further particles as can be described using the Bethe-Bloch Formula (see 3.3). These particles again interact with the material, creating a shower of particles. The calorimeter is designed to absorb this shower, converting the energy into light (in scintillators) or charge (in ionisation detectors), which is then collected and measured [25]. The total signal is proportional to the energy of the original particle, allowing for precise particle energy reconstruction as per the Shockley-Ramo-theorem [26, 27]. Calorimeters are

typically divided into electromagnetic and hadronic types, optimised for measuring electrons/photons and hadrons, respectively. Generally, hadronic showers are more complex and significantly longer due to the large plethora of particles and interaction mechanisms as well as being able to contain itself an electromagnetic shower within.

4. The ITk Upgrade

As part of the Phase II upgrade during the third long shutdown of the LHC (LS3), scheduled for 2026-2028, the ATLAS tracking detector will transition from the current Inner Detector (ID) system to a new all-silicon Inner Tracker (ITk) system. This upgrade is necessary to accommodate the projected increases in luminosity, pile-up, and radiation levels, as well as to replace degraded sensors. The ITk system will offer tracking coverage up to a pseudorapidity of $|\eta| \leq 4$ and will utilise, among others, pixels with a $50\,\mu m \times 50\,\mu m$ footprint, covering a total combined area of approximately $13\,m^2$ [2].

4.1. General Structure

The full structure of the ITk will consist of approximately 9164 modules [28] arranged in a nested barrel geometry, complemented by a series of endcap disks [29], ensuring complete coverage up to $|\eta| = 4$. A cross-sectional view of the planned module arrangement is presented in Figure 4.1.

The barrel section of the ITk comprises five cylindrical layers of pixel modules. These modules are mounted on lightweight mechanical support structures known as staves, which are, in turn, attached to longitudinal carbon-fiber-reinforced elements that form the structural spine of the barrel. This design guarantees mechanical stability under thermal and mechanical stress. Each stave houses multiple quad modules mounted on both sides to maximise spatial efficiency.

A key feature of the ITk design is its inclined geometry in the barrel section. Unlike the flat orientation of sensors in the current Pixel Detector, the modules in the ITk barrel are tilted with respect to the beam axis, particularly in the outer layers. This design enhancement improves coverage, especially for tracks at higher pseudorapidity. The inclination increases the effective path length of traversing particles within the sensor, thereby enhancing hit efficiency and spatial resolution for shallow-angle tracks [2].

The endcap region consists of a series of concentric disks, each populated with pixel modules mounted on wedge-shaped support structures known as petals. This arrangement ensures hermetic tracking coverage in the forward region, where track density is highest

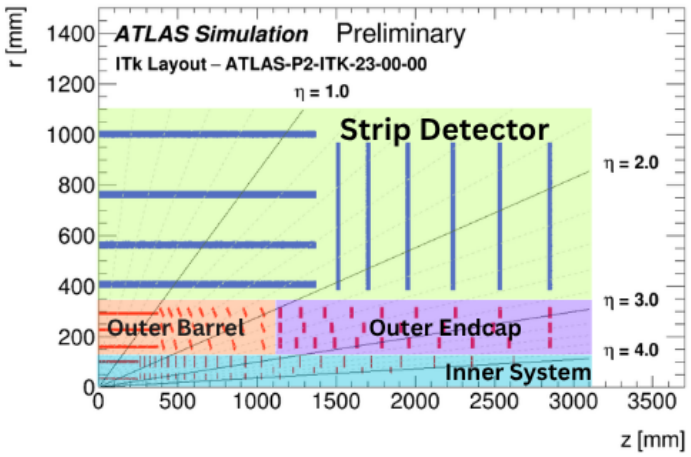

Figure 4.1.: A cross-sectional view of the updated ITk layout. Only one quadrant is shown. Based on [28].

due to the boosted topology of LHC collisions.

The ITk Strip Detector, by contrast, features larger-area modules and longer sensor strips optimised for tracking in lower-occupancy regions, with separate barrel and endcap layouts tailored for coarse-grained but efficient reconstruction.

The number of pixel hits per track is highly dependent on the track's pseudorapidity η. As illustrated in Figure 4.2, the inclined layout and denser layering in the forward region help maintain high hit multiplicity even for tracks with $2.5 < |\eta|$. This capability is essential for preserving the ITk's excellent pattern recognition and track reconstruction performance in the high-pile-up environment anticipated during the HL-LHC era.

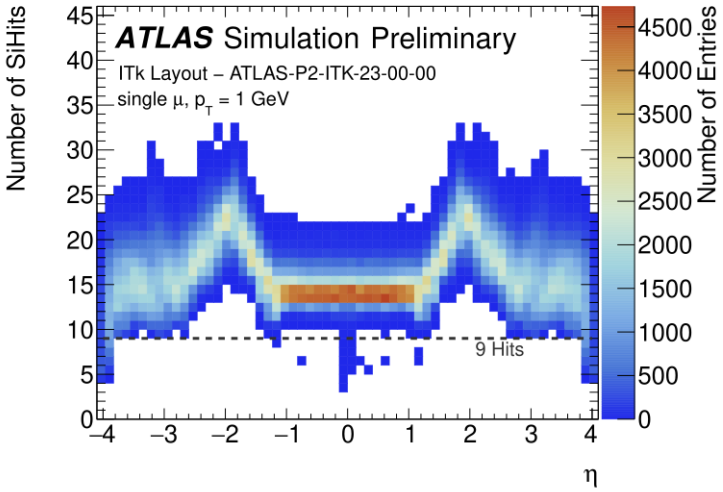

Figure 4.2.: Expected hit coverage of the updated ITk layout for varying pseudorapidities given a single muon sample event. Source: [28]

4.2. ITkPix Quad Modules

The pixel modules in the ITk system are based on radiation-tolerant silicon sensor technologies and are optimised for high spatial resolution and fast readout to handle the dense hit environment of the HL-LHC. They are specifically designed for the expected occupancy and radiation levels of their respective detector regions, with pixel pitch and readout granularity adapted as needed. The modules primarily utilise n-in-p type silicon detectors, featuring 384×400 individual pixels per front-end chip, resulting in an effective resolution of approximately 1.3 Gpx. The hybrid pixel detector modules consist of a single monolithic silicon sensor that is bump-bonded to four individual RD53 front-end (FE) chips. The FE chips are arranged in a 2×2 configuration and are responsible for analog signal amplification, digitisation, and zero suppression [30]. The sensor and FE chips together form the bare module, which is glued to the back side of a flexible printed circuit board (flex PCB). Electrical connections between the flex and the front-ends are established using 25 µm diameter wire bonds that extend along the module's entire edge. The flex PCB houses two connectors for power and data readout, as well as passive components such as decoupling capacitors to ensure signal integrity.

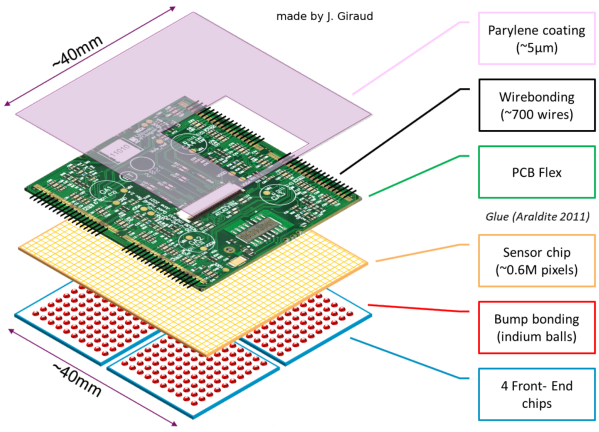

Figure 4.3.: Annotated schematic of the different layers composing a single quad module. Missing in this representation are the canopies (present only on outer barrel modules), attached onto the PCB flex to shield wire bonds below. Source: [31]

The chipset discussed in this thesis is the RD53B (also known as ITkPixV1.1), which represents the second generation of the RD53 family. The RD53A serves as a half-scale demonstrator developed to test various designs and architectures, acting as an R&D prototype. The RD53B provides a full-scale backbone for further testing and verification with experiment-specific front-ends (ATLAS and CMS). The RD53C (also known as ITkPixV2) is the final production version that incorporates many hardware fixes from the previous

generation [32].

During production and testing, the quad modules are placed onto a mechanical carrier to ensure mechanical stability throughout assembly, operation, and shipment.

In the final assembly phase, the modules are mounted to carbon-composite-based load structures referred to as Loaded Local Supports (LLS), which also feature a thermal connection to a cooling system [33]. Along these LLSs, modules are connected in serial power chains to minimise cabling, since such a configuration necessitates only one current source per serial chain.

5. Module Quality Control (QC)

As there is no viable method to service modules once integrated into the final ITk system, their functionality must be verified before assembly to ensure a usable and functional lifespan of at least 10 years. The Module Quality Control tests comprise a series of analyses and procedures performed on every module to determine whether it functions within acceptable limits. This allows for the identification and exclusion of malfunctioning modules prior to integration into the final build. The fraction of modules certified for use out of the total production volume is known as the yield, which in turn defines the required overproduction needed to reach the target of approximately 8372 modules for the ITk pixel subsystem [34]. The QC process described here reflects the procedure at the time of writing this thesis. It may not be final, as, despite the project transitioning from pre-production to production, ongoing improvements and refinements to the QC workflow continue to be proposed and implemented.

5.1. QC Process Overview

The local processing workflow for modules received in Göttingen is illustrated in Figure 5.1. Upon arrival, each module undergoes an initial visual inspection to identify any signs of damage incurred during transport or earlier manufacturing steps. After coating, the parylene de-masking process exposes the electrical contact pads, pickup points, and the full backside of the module for further testing. Parylene masks are applied beforehand to protect the board and to prevent coating of electrically active or contact-critical areas.

Subsequently, the Outer Barrel Wire Bond Protection (OBWBP) is installed. This involves gluing protective canopies onto the printed circuit board (PCB) to shield the delicate wire bonds on the sides from mechanical damage during handling and operation. After OBWBP installation, a second visual inspection is performed to verify correct placement and adhesion, followed by a metrological assessment.

Once these preparatory steps are complete, the module enters the electrical QC stage. This begins with a basic functional test to check for short circuits or obvious electrical defects. To assess robustness against thermal stress-expected during ITk operation, the

module is subjected to a series of thermal cycles, simulating repeated transitions between +40 °C and −45 °C.

Following thermal cycling, the module undergoes a final series of QC measurements. These include a warm electrical QC test at room temperature to validate basic functionality and a cold electrical QC test at the operational temperature of −15 °C, during which a source scan is performed to assess the module's response to incident radiation. The entire QC process concludes with final metrology to ensure that flatness has been achieved, enabling proper integration into the designed truss structure. These measurements are critical for ensuring the long-term reliability and performance of modules in the ITk detector environment.

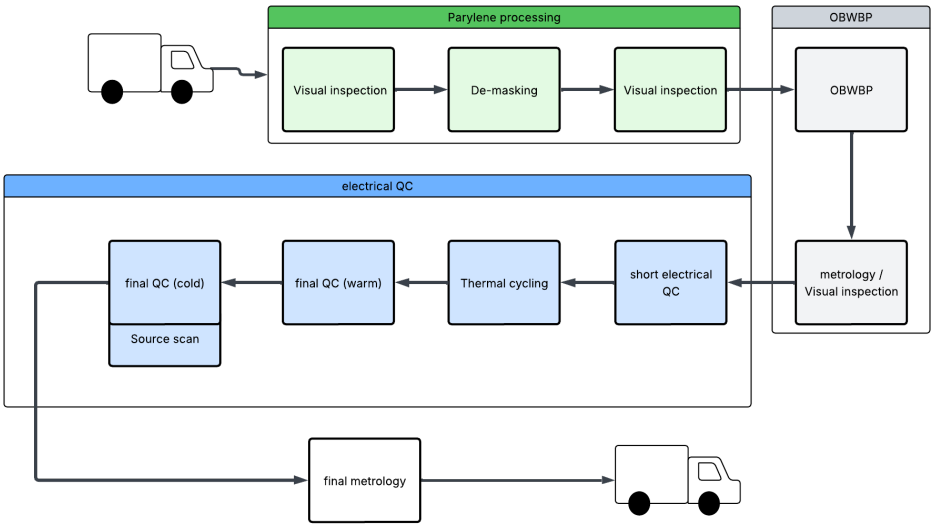

Figure 5.1.: Flowchart overview of the module processing in Göttingen. Excluding the last metrology step, the entire process can be segmented into a parylene processing step, an Outer Barrel Wire Bond Protection (OBWBP) step, and an electrical QC procedure. The order of operations for the electrical QC and final metrology can be arbitrarily swapped.

5.2. Electrical QC Tests & Procedure

The electrical QC tests can broadly be categorised into two groups:

1. Electrical characterisation measurements verifying key metrics and electrical behaviour.

2. Functional scans using YARR (further detailed in section 6.2.2) to evaluate data-taking capabilities via diagnostic scans, calibrations, and tunings.

A schematic overview is provided in Figure 5.2.

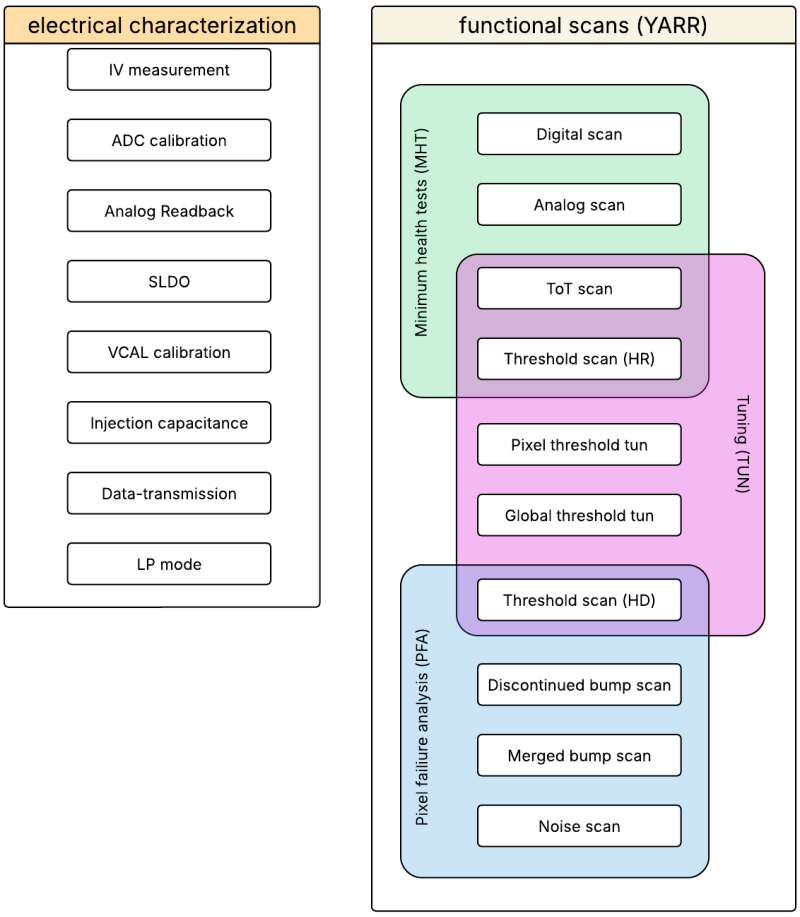

Figure 5.2.: Overview of electrical characterisation measurements (left) and YARR-based functionality scans (right) executed during a single electrical QC run. The three base routines - MHT (minimum health test), TUN (tuning), and PFA (pixel failure analysis) each share some scans with one another. Typical execution order is moving from top to bottom.

5.2.1. Electrical Characterisation

IV Measurement The IV measurement characterises the current drawn as a function of the high-voltage (HV) bias. During an IV scan, the module's HV supply is ramped from 0 V to 200 V in 5 V steps, while the current is continuously measured shortly after stabilising at each voltage level. One of the main goals of the IV measurement is to detect damage to the module, which can manifest as an early breakdown or excessively high leakage current. A sample test output is given in Figure 5.3.

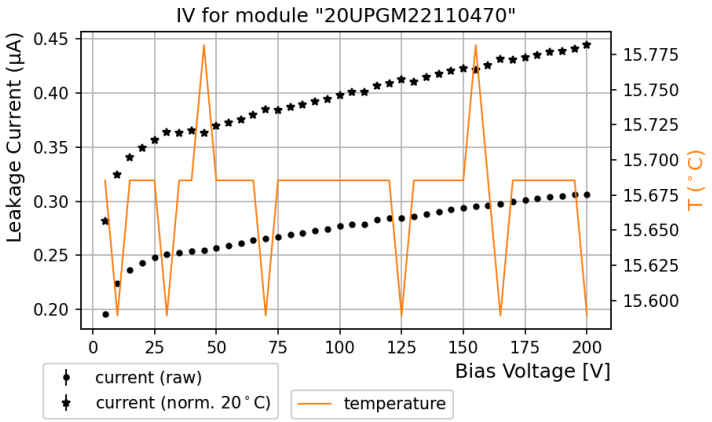

Figure 5.3.: Sample IV characterisation for module Q51 based on standard processing tools output.

ADC Calibration The ADC calibration verifies the accuracy of the internal analogue-to-digital (ADC) converters used to measure on-chip voltages and currents. This is done by applying a known voltage (typically via scanning the internal V_{cal} DAC) and comparing the ADC output to an external multimeter measurement. A linear fit extracts the ADC slope and offset, which are compared to acceptance criteria. This calibration is critical for all subsequent measurements relying on ADC readout and is stored in the chip configuration files.

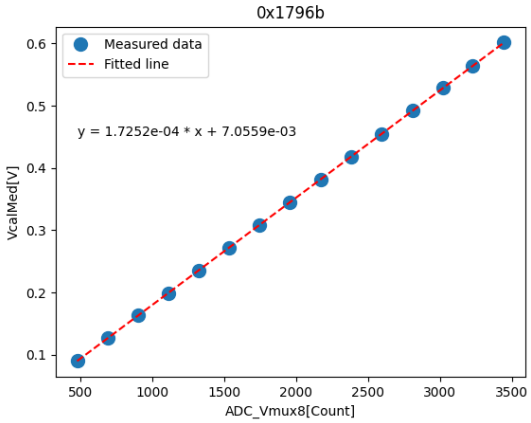

Figure 5.4.: Sample output of the ADC calibration of one FE as part of module Q49.

Analogue Read-back The analogue read-back test confirms the correct operation of internal voltage and current monitoring circuits. Using the calibrated ADC, various V_{MUX} and I_{MUX} values are read out to determine internal supply voltages (e.g., V_{DDA}, V_{DDD}),

Parameter	Analysis result	QC criteria	Pass
ADC CALIBRATION SLOPE	0.173	$[0.15, 0.224]$	True
ADC CALIBRATION OFFSET	7.0	$[-9, 31]$	True
ADC CALIBRATION LINEARITY	0.3	$[0.0, 4.0]$	True
ADC ANAGND30 MEAN	0.018	$[0.012, 0.023]$	True
ADC ANAGND30 STD	0.0	-	-

Table 5.1.: Summary of ADC calibration results of FE 0x1796b (part of module Q49).

reference voltages (e.g., V_{refA}, V_{refD}), and currents (e.g., input and shunt currents). Temperature sensors are also read out and validated. All measured values are compared to expected ranges to detect possible configuration or regulation issues.

V_{cal} Calibration This test characterises the internal DAC responsible for charge injection (V_{cal}). A scan over the DAC range is performed while monitoring the output voltage with an external multimeter. Slope, offset, and linearity are extracted and compared to expectations. Both small and large range settings are tested. Accurate V_{cal} calibration is essential for threshold tuning and charge injection. A sample output is presented in Figure 5.5 and Table 5.2.

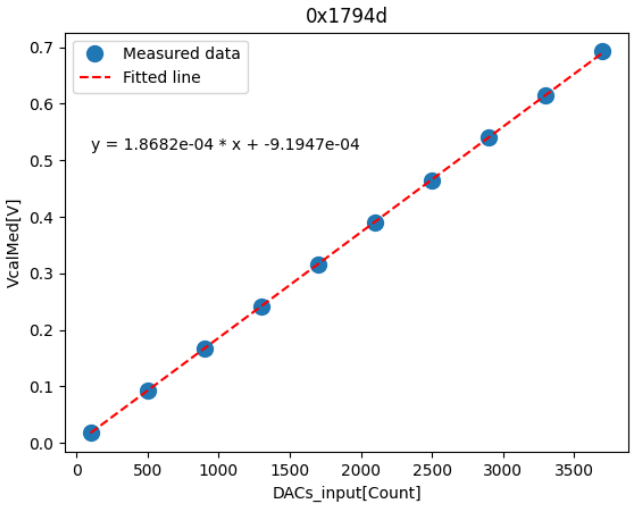

Figure 5.5.: Measurements of the V_{cal} calibration procedure with the measured voltage as a function of the specific DAC input value for a single FE of the module Q49 in the medium DAC range.

Injection Capacitance This test measures the on-chip injection capacitor, which, combined with the V_{cal} DAC, defines the injected charge during calibration pulses. The

Parameter	Analysis result	QC criteria	Pass
V_{cal} MED SLOPE	0.19	$[0.16, 0.24]$	True
V_{cal} MED OFFSET	-1.0	$[-23, 17]$	True
V_{cal} MED LINEARITY	1.03	$[0.0, 4.0]$	True
V_{cal} MED LINEARITY SMALL RANGE	0.57	-	-
V_{cal} HIGH SLOPE	0.19	$[0.16, 0.24]$	True
V_{cal} HIGH OFFSET	-2.0	$[-23, 17]$	True
V_{cal} HIGH LINEARITY	0.52	$[0.0, 4.0]$	True
V_{cal} HIGH LINEARITY SMALL RANGE	0.43	-	-
V_{cal} HIGH SLOPE SMALL RANGE RATIO	0.5	$[0.49, 0.51]$	True
V_{cal} MED SLOPE SMALL RANGE RATIO	0.5	$[0.49, 0.51]$	True

Table 5.2.: Results of the V_{cal} calibration for FE 0x1794d (part of Q52).

measured value is compared against expectations (target: $7.87 \pm 1.13\,\text{fF}$)[35]. Accurate capacitance measurement is crucial for interpreting threshold and noise in elementary charge units.

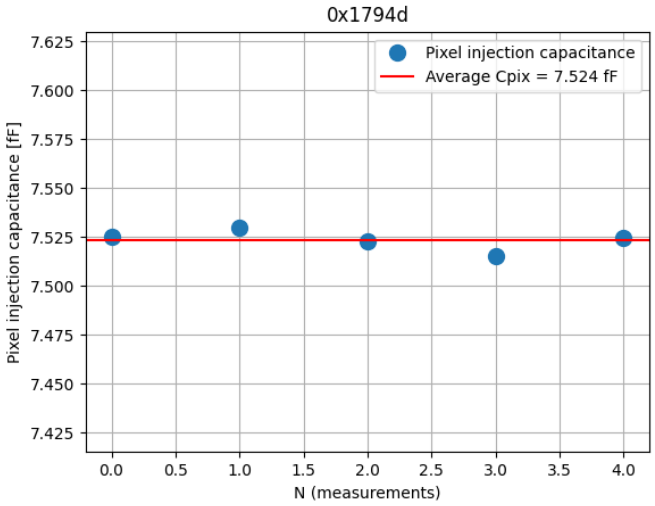

Figure 5.6.: Results of the Injection Capacitance measurement for an FE from module Q52. Overall, five measurements were taken and the average used to satisfy the QC criteria.

Data Transmission The data transmission test evaluates the quality and reliability of the high-speed communication links between the module and the readout system. This is done via an eye diagram measurement (further detailed in the upcoming section).

Low Power (LP) Mode The LP mode test checks the module's functionality when operated under reduced power conditions, as required during integration and wiring into the system after installation. The module is powered with the nominal LP current, and key voltages are measured. These include the analogue and digital supply voltages, offset voltages, and shunt currents. Additionally, data transmission is tested in LP mode by running an LP digital scan and confirming connectivity.

SLDO Qualification The Shunt Low Dropout (SLDO) regulator qualification tests the internal voltage regulation mechanism of each front-end chip. The module is powered with a range of input currents, and the input voltages, supply voltages, and shunt currents are recorded. This test ensures stable and predictable voltage regulation across the module's operating range.

5.2.2. YARR Scans

A YARR (further detailed in section 6.2.2) scan is defined via a descriptive JSON file containing data-taking and plotting logic. The procedure consists of nested loop operations for injecting charges into the analogue or digital parts of the detector while applying varying pixel masks. Three key scan routines are part of the QC process: the Minimum Health Test (MHT), the Tuning Test (TUN), and the Pixel Failure Analysis (PFA). These stages, as visualised in Figure 5.2, test the module's health, tuning parameters, and pixel-wise performance.

Eye Diagram

The eye diagram is a digital diagnostic tool used to assess the signal quality of high-speed serial data links. By overlaying multiple signal cycles, a characteristic 'eye'-shaped plot is formed.

In YARR, the eye diagram evaluates communication between the RD53B chip and the read-out FPGA (Field Programmable Gate Array) (e.g., KC705) over Aurora links. These links operate at gigabit speeds, requiring precise timing. The de-serializer delay is systematically scanned, and for each delay setting, the number of received non-idle frames is counted. Comparing this to the expected frame count yields a link quality metric:

$$S_{\text{Quality}} = \frac{\log \frac{N_{\text{expected}}}{|N_{\text{measured}} - N_{\text{expected}}|}}{13} \tag{5.1}$$

For perfect signal integrity ($N_{\text{measured}} = N_{\text{expected}}$), the expression diverges towards infinity. To keep the metric bounded and easy to interpret, S_{Quality} is capped at 1, which represents

a perfect or near-perfect link quality.

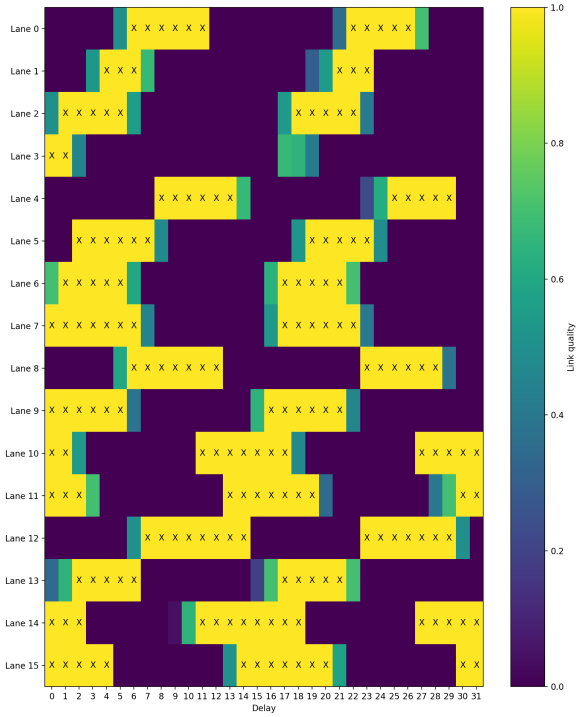

Figure 5.7.: Visualisation of the YARR-based eye diagram. For each link lane (y-axis), the link quality is shown for different delay settings.

For every link, the centre of the widest continuous region with perfect link quality is chosen as the optimum delay setting to be stored in the controler configuration file and later applied to subsequent scans. Due to the strong dependence of the signal quality on the exact hardware connection, it is sensible to rerun an eye diagram after every change of cables, adapters, or similar. Failing links may indicate hardware issues, primarily connection losses, as well as a misconfigured link speed or generally poor signal quality.

Digital Scan

Digital scans test the logic functionality of the front-end chip, including address decoding, command handling, and signal routing. Failing pixels in these scans may indicate faulty or misconfigured pixels, communication issues, or logic faults.

Analogue Scan

This scan verifies the analogue signal chain-amplification, discrimination, and signal uniformity across the pixel matrix. Results are used to identify noisy or non-responsive pixels. Known charges are repeatedly injected into the pixel matrix and resulting hits

are registered. The number of hits for a given pixel must closely match the number of injected charges.

Threshold Scan

The threshold of a given pixel is the minimum amount of charge required to register as a hit in the onboard electronics (discriminator). The duration that this threshold is surpassed is the time over threshold (ToT) and is directly proportional to the induced charge. The threshold scan is used to calibrate this value for every pixel using the internal calibration circuitry to inject known charge amounts while measuring the pixel response. This procedure can detect noisy and entirely dead pixels. In operation, the threshold value helps suppress undesired signals caused by noise, leakage currents or a number of other external influences on the sensor, in an effort to isolate the desired signal of a given interaction.

Merged & Discontinued Bump Scan

The merged and discontinued bump scan is used to assess the physical bump-bond connectivity between the actual sensor and its readout chip. In a properly assembled module, each bump pad connects a sensor pixel to its corresponding front-end electronics channel. However, defects during the flip-chip bonding process can lead to merged bumps (where two or more pixels are shorted together) or discontinued bumps (where a pixel is disconnected and does not respond to signals).

This scan injects charge in patterns designed to isolate and detect such anomalies. By analysing hit maps and comparing the activated pixels to the expected geometry, merged or missing connections can be identified.

Tuning Scans

Tuning scans aim to calibrate the analogue and digital front-end parameters on a per-pixel basis to achieve uniform detector performance. Parameters such as threshold, time over threshold (ToT) response, injection capacitor gain, and feedback current are subject to local variations due to production tolerances. These variations, if left uncorrected, can lead to inconsistent signal detection and affect overall detector resolution and noise performance.

The tuning procedure involves multiple iterations of threshold and ToT scans, during which configuration parameters (such as DAC settings for thresholds and feedback) are adjusted. The goal is to equalise the detector response across all pixels, setting the

threshold to a target value and calibrating the ToT to correspond to specific charge values. Well-tuned modules display narrow threshold and ToT distributions and minimal spread in pixel performance. Tuning is a critical step in module qualification ensuring uniformity.

6. Test Setup

6.1. Hardware

To conduct the tests mentioned earlier (see section 5.2.1 and 5.2.2), specialised equipment and a comprehensive testing setup are required.

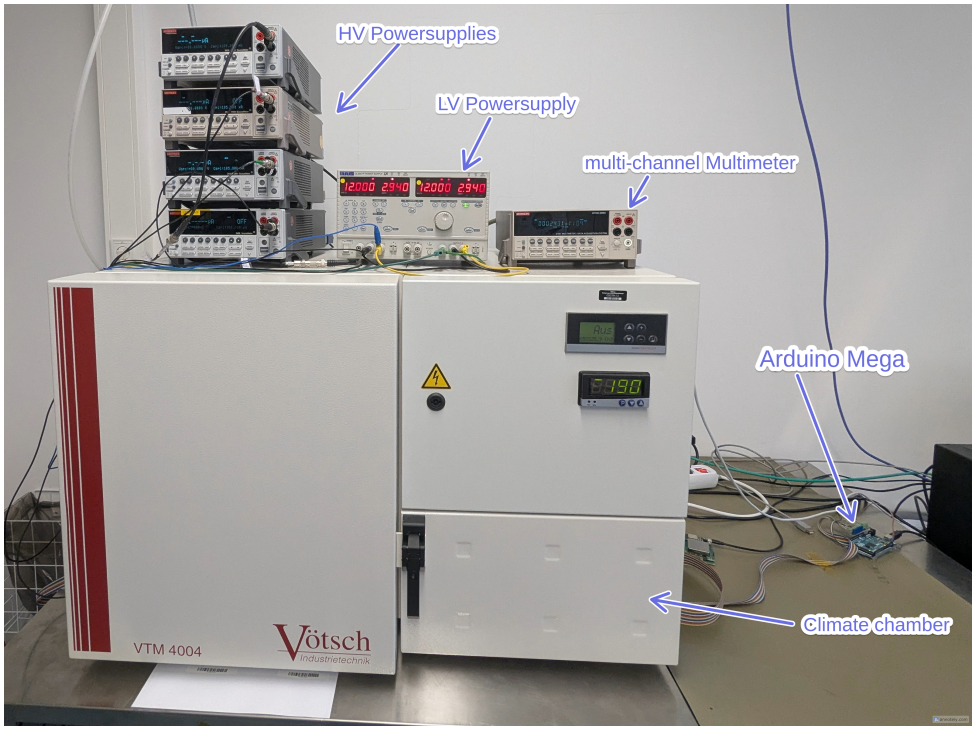

Figure 6.1.: Utilised testing setup after upgrades and changes, including the climate chamber (bottom), the Keithley 2410 HV power supplies (leftmost stack on top), the LV PS (centre top), and the multimeter (right top) along with the Arduino Mega (on the far-right side of the table).

An overview of the entire test setup is presented in Figure 6.1. For electrical QC, each quad module connects to a power and a data adapter PCB through two flex cables (further visible in Figure 6.3 front and rear of the mounting plate). These PCBs link the module to the PCIe card (via a DisplayPort cable) for data acquisition, an Arduino (for temperature monitoring), a multimeter (for onboard electrical checks), and low voltage/high voltage

(LV/HV) supplies (providing the power for operation and bias voltage).

The modules reside within the climate chamber for cooling, which helps to prevent thermal stress and potential failures. To avoid condensation, the chamber is continuously flushed with dry air. A network of software interlocks continuously monitors the system to prevent common failure modes, including overheating and the risk of condensation.

6.1.1. Climate Chamber

The testing setup employed throughout this thesis revolves around a climate chamber (Vötsch VTM 4004), within which, initially, up to two, and now up to four quad modules can be placed. It is based on an earlier configuration established in the works of Niklas Grün [36] and Yusong Tian [37], which provide more detailed descriptions of certain aspects of the infrastructure. In this configuration, the modules are cooled by the surrounding air, with the climate chamber facilitating the cooling of the air itself to maintain a stable temperature environment. To ensure a homogenous temperature, a fan is used to circulate the air within the chamber. However, an alternative approach is utilised in the new testing box, where direct cooling of the modules is achieved using Peltier elements. This method allows for more efficient and localised cooling, thereby enhancing the thermal management of the modules during testing and improving overall performance.

Each module is connected to the readout PC's FPGA card via a DisplayPort cable through a corresponding data adapter PCB. Additionally, the modules are connected to a power adapter PCB that interfaces with an LV power supply, delivering 5.89 A at a maximum voltage of 3 V per quad module, alongside an HV power supply capable of delivering up to 200 V. While the former is responsible for supplying operational power to the quad module, the latter is required to set the bias voltage of the sensor.

Initially, the setup required two separate LV power supplies to handle two individual quad modules, thereby providing an independent power supply for each quad module. However, the current configuration allows all four quad modules to be wired in a serial chain powered by a single supply. This modification reduces hardware setup complexity and minimises cabling while also testing the efficacy of the serial powering feature.

6.1.2. Sensors & Labremote

The onboard chip temperature of each quad module is monitored from a passthrough connection of an on-chip thermal sensor. This sensor is linked on the power adapter board to an Arduino Mega. The thermal data from the modules NTCs, along with readings from an independent PT1000 temperature sensor and I2C-based SHT85 temperature and

humidity sensor within the climate chamber, are written via the Arduino Mega to a local PC through a USB serial connection. From there, the data is parsed and uploaded through Labremote to a centralised InfluxDB, enabling close to real-time monitoring (typically with a delay of less than 2 s).

Additionally, environmental data from the room, such as temperature and particulate matter counts of various sizes, are measured and recorded in the same database. The voltage and current from connected power supplies (LV and HV) are also logged into the local InfluxDB through the connected GPIB interface.

6.1.3. Database and Grafana

The overall system status is visualised through a series of Grafana dashboards that display temperatures, humidity levels, voltages, and other custom fields as time-series plots and gauges (see Figure 6.2). This visualisation aims to provide an intuitive overview of the system's status and is a crucial tool when running and monitoring electrical QC scans.

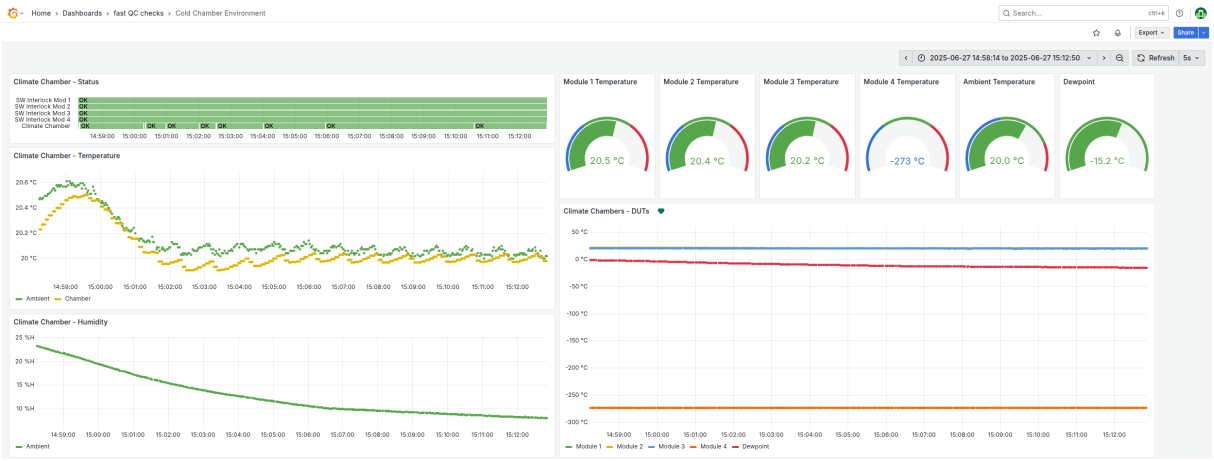

Figure 6.2.: Grafana dashboard to monitor environmental factors including relative humidity and temperatures. Further dashboards include those to monitor power and progress/status.

An active notification system is established to proactively alert users in case the system reaches a critical state, such as a module approaching unsafe temperatures or at risk of condensation due to a higher dew point. These warning messages are sent by Grafana to a designated Slack group, allowing for a prompt and efficient response to maintain system integrity and avoid compromising the functionality of the modules.

Upon completion of a test or scan, the results can be uploaded to a 'localdb' for storage and approval, after which it will be passed on to the production database. Within the

localdb, all modules, their components, original location on the production wafer, as well as a historic record of all scans and tests run on any particular module can be viewed.

6.1.4. Interlock Systems

In order to prevent damage to a module or the occurrence of unsafe testing conditions, continually running software interlocks are employed. Each quad module is monitored by a dedicated interlock process that tracks its onboard temperature and dew point, calculated from the thermal data stored in the central database instance.

If an interlock condition is triggered due to overheating or a risk of condensation, the system swiftly enters a safe state.

An interlock process routinely checks that the monitored parameters remain within limits defined in a configuration file. These limits include:

- **Temperature thresholds:**
  - Absolute upper bounds for module temperature (40 °C)
  - Minimum ΔT between the module and the environment (dew point margin) (2 °C and 5 °C for error state and warning, respectively)
- **Current thresholds:**
  - Maximum allowed bias current
  - Maximum acceptable current variation and fluctuation
- **Timeouts:**
  - Maximum allowed age of the latest sensor reading
  - Warning and critical thresholds for data freshness (20 s and 40 s, respectively)

When an interlock condition is triggered, the corresponding power supplies are ramped down and subsequently switched off. A file lock is also released to signal to other software components that an interlock is active. In cases of dew point-triggered interlocks, the chamber is brought to a safe state by raising its internal temperature to 25 °C.

6.1.5. Mounting Plate

To facilitate testing of four quad modules within the climate chamber, a custom 3D-printed mounting plate was designed and fabricated by the author in the course of this

thesis. This upgrade was essential for organising the modules, adapter PCBs, and cabling within the limited space of the climate chamber.

Throughout this thesis, frequent thermal issues were observed in pre-production modules, which often exhibited suboptimal thermal behaviour. Some modules overheated even when operating near the minimum temperature of $-35\,°C$, highlighting the necessity for robust cooling and monitoring strategies. The mounting plate was designed with perforations on every flat surface to enable better movement of air, the coolant, around the modules while still remaining rigid enough to withstand daily wear and tear. Unlike the previous dual module setup in the climate chamber, in which modules were simply laid flat onto the rack without any fixation, the mounting plate provides mounting pins on which a module can be placed. This prevents the modules from moving around and subsequently knocking loose any cables during operation, as well as raising a module to allow for more air circulation directly below the metal carrier, the main heatsink.

The part was manufactured using a common fused filament fabrication 3D printer with PLA (polylactic acid) plastic and a layer height of $0.2\,\mathrm{mm}$ and 20% gyroid infill. The design was optimised for mechanical stability and airflow while ensuring compatibility with the existing infrastructure inside the climate chamber.

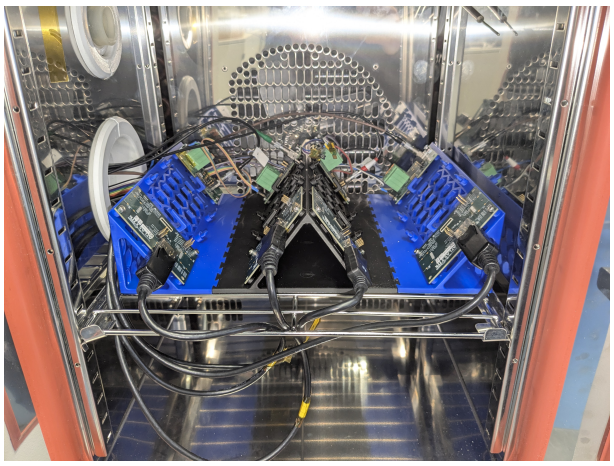

Figure 6.3.: Inside of the climate chamber. Quad modules are inserted onto the visible pins on the mounting plate and connected via the flex cables to the front and rear adapter PCBs. Cables are passed through the hole in the climate chamber on the left.

New QC Box To accommodate the projected QC workload, a new and streamlined testing configuration is currently being built and finalised in parallel with this thesis project. The newly assembled *QC Box* is designed to test up to four modules simultaneously, and it is functionally similar to the setup utilised during the course of this thesis

while also improving upon it [38]. The experiences gained from the climate chamber setup, particularly in the area of parallelising various scans, will be directly transferable to the new testing box, playing a crucial role in optimising the QC procedure and assuring adequate throughput.

6.2. Software

Control over the hardware components is distributed among several software systems, including Labremote, YARR, and ModuleQCTools. While the former provides monitoring data as previously mentioned through interfacing with an Arduino Mega, the latter two are for data readout and module measurements and are thus crucial for the electrical QC.

6.2.1. Module QC Tools

The `module-qc-tools` repository is a Python-based suite of scripts and tools for running QC measurements on ITkPixV1.1 and ITkPixV2 modules. Supported tests include: ADC calibration, analogue readback, data transmission, injection capacitance, IV measurement, low power mode, SLDO qualification, and V_{cal} calibration as specified in section 5.2.1. The measurements are generalised and controled by single scripts, with the hardware and control methods specified in a central configuration file.

6.2.2. YARR

The **Y**et **A**nother **R**apid **R**eadout (YARR) software framework is a readout system developed for the configuration, control, and data acquisition of hybrid pixel detector modules.

YARR provides a flexible and extensible environment for interacting with front-end electronics, particularly the RD53 family of chips, including the RD53A, RD53B, and RD53C chipsets, used in ITk pixel modules. Its core functionalities include:

- **Chip and module configuration:** Through JSON-based configuration files, YARR enables detailed control of chip-level parameters, global registers, and module-level settings.
- **Scan and test automation:** YARR supports a wide variety of scan types, such as threshold scans, noise scans, and digital tests, which are essential for characterising detector performance during module production and qualification.

- **Data acquisition (DAQ):** The framework interfaces with FPGA-based hardware platforms (e.g., Xilinx KC705, VCU118) to manage real-time readout of pixel data and buffering of event information.
- **Parallelisation and scalability:** YARR can be configured to operate multiple modules simultaneously, an essential feature for scaling QC operations to production levels. This feature is to be put to the test.

YARR is written in C++ with Python bindings and uses descriptive JSON files to define scan logic and hardware configurations. It is co-developed by the ATLAS ITk community and is designed to adapt to evolving detector and hardware requirements.

The YARR Firmware is flashed onto the DAQ PC's Xilinx KC705 FPGA card using Vivado Lab software, while the YARR software package manages and coordinates scanning and testing procedures as detailed in section 5.2.2.

7. Feasibility and Performance of Parallelised Module QC

The goal of this thesis is to evaluate the feasibility and viability of parallelising electrical quality control tests for silicon pixel detector modules. As most tests are executed using the YARR software framework, a central focus is placed on assessing the degree to which YARR-based scans can be parallelised. In total, six quad modules were available for testing during this thesis: Q28, Q29, Q49, Q51, Q52, and Q55. An additional seventh module, Q17, was used exclusively for the final scan series[1] Module Q28 was found to be faulty from the beginning and could not establish a functional link during eye diagram scans. As such, it was excluded from all subsequent tests.

To quantify the degree of parallelisation, we define the parallelisation percentage p as the normalised duration of a parallel run:

$$p = \frac{T_n}{T_1} \cdot \frac{1}{n} \tag{7.1}$$

Here, T_1 is the scan duration for a single module, and T_n is the total duration when testing n modules in parallel.

The uncertainties here are given through Gaussian error propagation with the standard deviation of a set of time measurements as the error:

$$\sigma_P = \frac{1}{n}\sqrt{\left(\frac{\sigma_{T_n}}{T_1}\right)^2 + \left(\frac{\sigma_{T_1} \cdot T_n}{T_1^2}\right)^2} \tag{7.2}$$

7.1. Electrical Characterisation

The electrical characterisation tests rely on an external multimeter to measure basic electrical properties such as current draw, voltage stability, and power-up behaviour. As

[1]The QXX identifiers are only abbreviated codenames for the longer, more descriptive identifiers. These are 20UPGM22101121, 20UPGM22101122, 20UPGM22110565, 20UPGM22110470, 20UPGM22110471, 20UPGM22110518, and 20UPGM22110467, respectively.

these instruments are available on a per-module basis, a high degree of parallelisation can be expected.

7.1.1. IV Measurement

The IV (current-voltage) measurement only requires control over each module's high-voltage (HV) power supply. As each test slot is equipped with its own HV supply, a high degree of parallelisation is possible. Modules Q49, Q51, Q52, and Q55 were installed in slots 1 through 4, respectively, with the climate chamber set to 15 °C.

Measurements were launched in parallel using Python's multithreading library to run the *module-qc-tools* IV measurement script. For each test run, a random subset of the installed modules was selected, and each corresponding IV scan was executed in a separate thread. The time from the start of the first thread to the end of the execution of the last thread was recorded for each test run. Each configuration was tested in six independent repetitions. The resulting duration times versus the number of active modules are shown in Figure 7.1, with the error assumed to be of a statistical nature, derived from the standard deviation across all respective repetitions. A sample time series of a single test run with all four quad modules enabled, as displayed in Grafana, is shown in Figure 7.2.

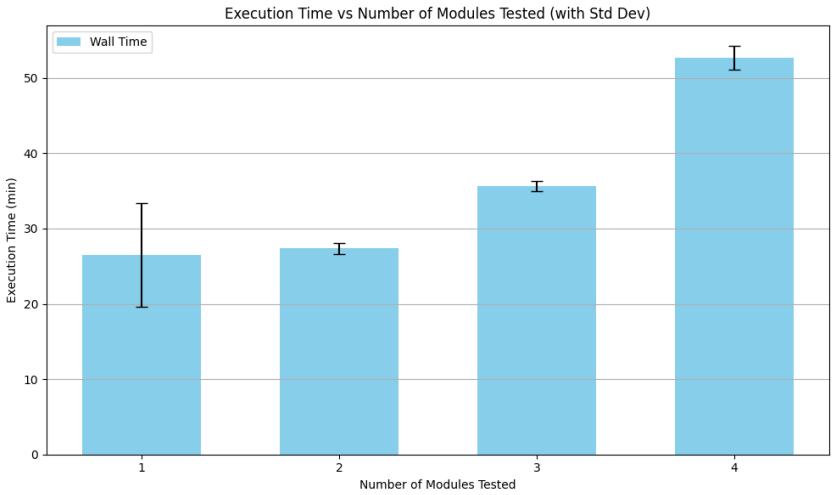

Figure 7.1.: Total execution times for running the IV measurement on one, two, three, and four quad modules simultaneously using the varying HV power supply. No linear fit is shown, as the data exhibits clear deviations from linear behavior and the reduced chi-squared value of a potential linear regression ($\chi^2_{\text{red}} \approx 38$) indicates a poor fit quality.

As can clearly be observed in Figure 7.2, there are significant timing inconsistencies between different slots tested. This was traced back to the different models of HV power

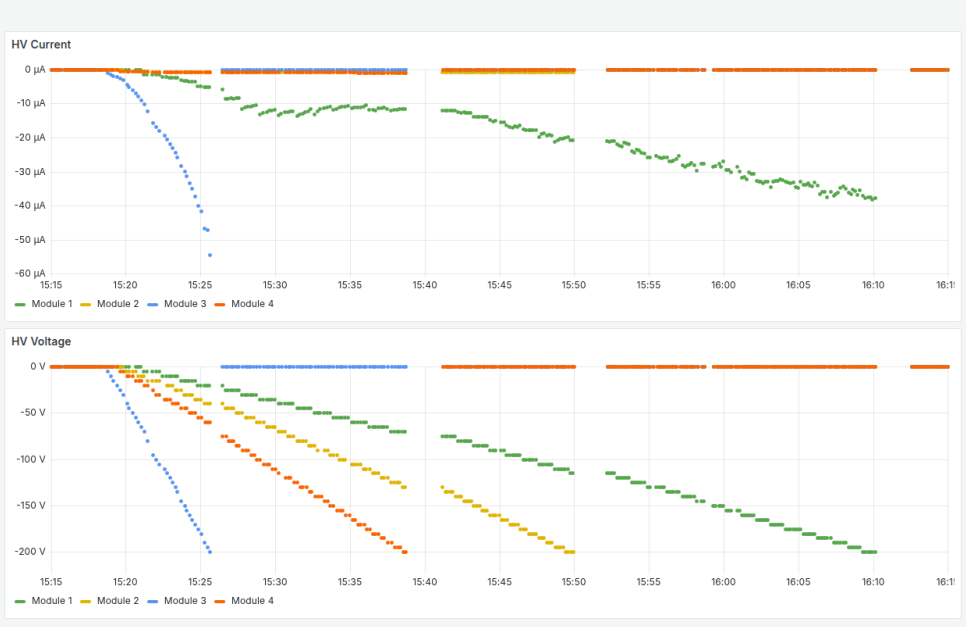

Figure 7.2.: Sample time series plot of the HV PS voltage and current for four quad modules running one IV measurement using different HV PS. Slots where no data is recorded correspond to a PS being in ramp down mode, blocking all other command executions.

supplies utilised (Modules 1, 2, and 4 are connected to SHQ 122M supplies while Module 3 is connected to a Keithley 2410). Additionally, it can be observed that during the ramp-down period after the maximum bias voltage is reached, the HV PS blocks all other processes (including data taking) running simultaneously until fully ramped down. While the SHQ 122M supplies take $\approx 2.3\,\text{min}$ each, the Keithley 2410 has a ramp-down period of $\approx 0.7\,\text{min}$.

The benchmarking procedure was repeated after modifying the setup to use four identical Keithley 2410 HV PS units, replacing the heterogeneous set of supplies used previously. The resulting test durations versus the number of modules are displayed in Figure 7.3, along with a time series overview of two test cycles using the uniform HV PS in Figure 7.4.

This switch to uniform HV PS shows a clear improvement in timing reproducibility across the different slots, as well as an overall reduction in testing time. A linear fit across these timings can be applied to get an approximation for the scan duration depending on the number of modules scanned, as given in Figure 7.3.

The new Keithley 2410 HV PS units achieve the set voltage increments faster and require shorter times to settle on the desired voltage level, leading to an overall reduction of the single-module test time from as long as $\approx 55\,\text{min}$ with the old setup down to merely $\approx 6\,\text{min}$ using the new HV PS for a single quad module. The degree of parallelisation

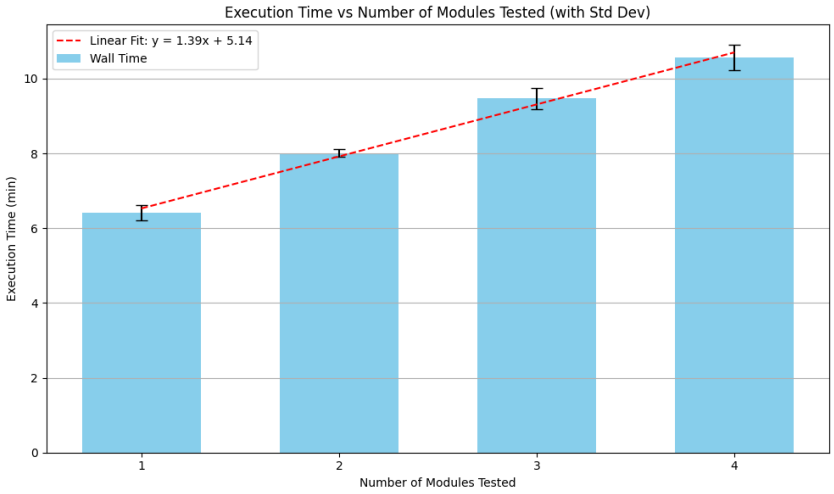

Figure 7.3.: Total execution times for running the IV measurement on one, two, three and four quad modules simoultaneously with identical Keithley 2410 HV PS. The fit is given as $y = (1.39 \pm 0.08)x + (5.14 \pm 0.08)$ with $\chi^2_{red} = 0.74$, indicating a good fit.

achieved with the upgraded setup for 2, 3, and 4 modules, respectively, is shown in Table 7.1. The error is given through a Gaussian error propagation:

# Modules	Degree of Parallelisation
2	$(62.4 \pm 2.2)\,\%$
3	$(49.2 \pm 2.2)\,\%$
4	$(41.2 \pm 1.9)\,\%$

Table 7.1.: Measured parallelisation percentage for IV scans using 2-4 modules.

7.1.2. Further Electrical QC Tests

Parallelising the further electrical QC tests, including ADC calibration, analogue readback, VCAL calibration, injection capacitance, data transmission, LP-mode, and SLDO yielded no usable results, as any parallelised scans exited immediately, leaving only one test running at a time. Across all remaining electrical QC tests, a common error scheme was observed, with the respective scans terminating when attempting to initialise a YARR instance. As no successful parallelised scan runs were feasible, no further data could be gathered and analysed.

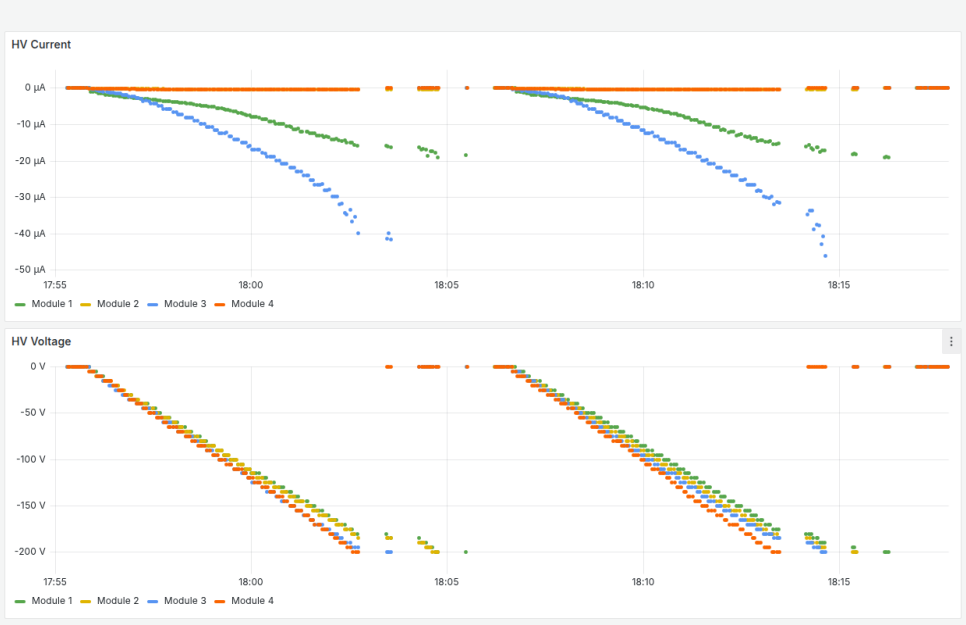

Figure 7.4.: Sample time series plot of the HV PS voltage and current for four connected quad modules running two IV measurements back to back using the Keithley 2410 PS. The durations lacking datapoints are those during wich a PS was in a ramp-down phase, thus blocking further command execution on the GPIB interface and halting all other running processes.

7.2. YARR-Based Functional Scans

This section systematically evaluates the parallelisability of the YARR-based functionality scans. All distinct scan types from the MHT, TUN, and PFA testing stages were considered and compared in a structured manner to assess their suitability for parallel execution. This evaluation forms a crucial basis for understanding potential bottlenecks and opportunities for optimisation in the upcoming quality control campaign. As opposed to the previously mentioned electrical characteristic tests, a test here does not require the careful synchronisation of multiple tools. Those tests typically involve coordinating several components, including a YARR instance, which prevents multiprocessing. In contrast, a single YARR instance can be called with multiple quad modules passed as arguments. This enables the processing of multiple modules at once and avoids the need to spawn multiple YARR instances.

7.2.1. Initial Tests and Software Verification

To validate the hardware setup and to gain familiarity with the test procedures, initial test scans were conducted on all available modules using the proven single-module con-

figuration. Modules Q29 and Q51 showed irregular scan behaviour, with error rates of approximately 4 out of the first 14 scans[2]. A selection of some of these scan results is presented in Section 5.2.2.

Subsequently, all core software components-including YARR, *module-qc-tools*, and supporting utilities-were upgraded to their latest stable versions, as recommended during a module QC coordination meeting. In parallel with the firmware upgrade, the link bandwidth was increased from 640 Mbps to 1280 Mbps in order to test the high speed data link at the speed required during operation.

To verify that the software and firmware upgrades did not introduce inconsistencies, comparative scans (limited to digital and analogue scans) were performed on identical modules before and after the upgrade. A pixel-wise difference between pre- and post-upgrade scan results was computed to confirm stable behaviour; ideally, the resulting difference map should be uniform. An illustrative example for module Q49 is shown in Figure 7.5. Overall, the scan outputs appear nearly identical, confirming the correct functionality of YARR version 1.5.4.

7.2.2. Scan Runtime

A central aspect of this thesis is the duration of a given scanning procedure. Throughout the initial investigations and preliminary tests, it became evident that the runtime of these scans can be measured and quantified in three distinct ways:

- **YARR log timing:** YARR records start and end timestamps within the `scanLog.json` file. The difference between these timestamps defines the total scan duration.
- **Stage timing:** Embedded stopwatch timers during scan execution, also stored in `scanLog.json`, yield individual durations for each scan stage (configuration, scan, analysis, and processing). These values provide insights into the duration of each component, and their sum yields the total scan time, but not the same value as the aforementioned.
- **External timing:** Measurement of total elapsed time via an external system timer for measuring the actual command execution time (e.g. implemented in Python).

These methods consistently report differing values for the same scan. External timing typically yields the longest duration, followed by the difference between start-end timestamps, while the sum of individual stage durations is consistently the shortest. For most

[2]Scan errors refer to failures reported by YARR, typically caused by poor signal integrity, faulty FE chips, or unstable configuration.

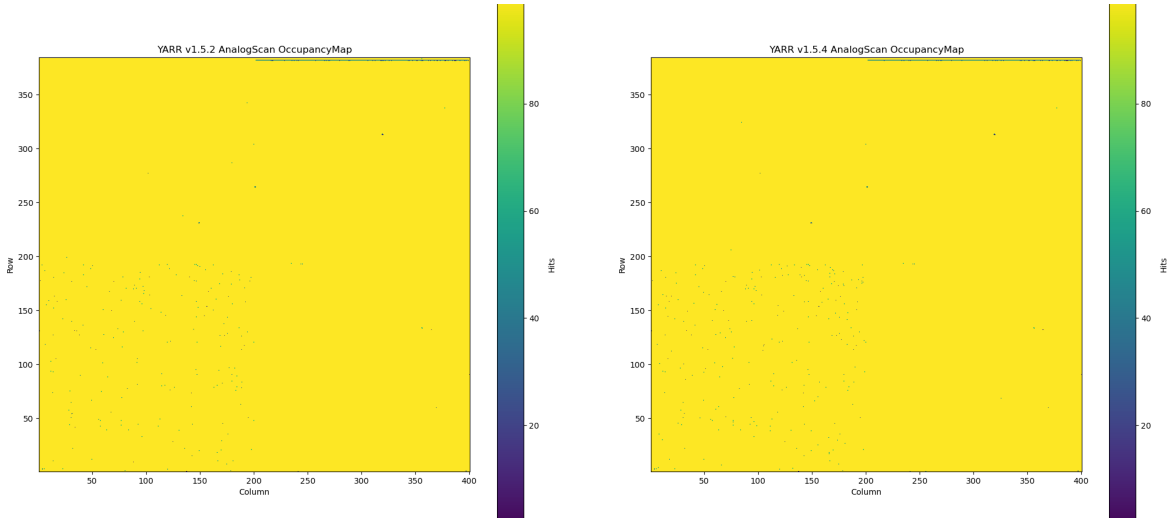

Figure 7.5.: Analogue scan occupancy map of module Q49 running YARR version 1.5.2 (top left), version 1.5.4 (top right), and the pixel-wise difference (bottom).

scans discussed in this thesis, all three timing methods were recorded. Unless otherwise noted, all subsequent scan timing analyses are based on the internal stopwatch timing to provide the most granular and consistent picture of scan execution times.

7.2.3. Front-End-Wise Scan Times

To assess the degree of parallelisation across different YARR scan types, dedicated tests were performed with 1, 2, 3, and 4 quad modules operated simultaneously. Modules Q17, Q49, Q51, and Q55 were placed in slots 1, 2, 3, and 4, respectively. These tests systematically varied the number of active front-end (FE) chips per module, evaluating configurations with 4, 8, 12, and 16 FEs. For each FE configuration, six random subsets out of the total 16 FEs were selected and activated via their corresponding configuration files. For every subset, all scan types were executed consecutively, and the command execution time was independently recorded for each scan and later re-associated with the corresponding run. The average duration of each scan stage-configuration, scan, analysis, and processing, as a function of the number of enabled front-end chips (FEs) can be evaluated individually for every scan type. For each scan stage, a linear relationship of the form

$$T = a \cdot n + b \tag{7.3}$$

is fitted, where T denotes the time duration, n the number of active FEs, and the fit parameters a and b represent the runtime per module and the constant overhead, respectively.

Representative examples of this behaviour are shown in Figures 7.6 and 7.7, which display the Analogue scan and Noise Scan, respectively. The left-hand panels show the average duration of individual scan stages with increasing FE count. The timing uncertainty is represented by the standard deviation across six repetitions per configuration. Systematic deviations stemming from clock resolution or hardware timing inaccuracies are considered negligible, as they are typically limited to the millisecond range and thus insignificant compared to statistical spread. The uncertainties of the linear fit parameters are provided as their variances, and the full set of fit results is summarised in Table B.3.

To further evaluate potential systematic discrepancies in the reported scan durations, the externally measured total runtime, the YARR-reported total time, and the sum of YARR-reported individual scan stage durations are compared. The right-hand panels of Figures A.1 illustrate these comparisons for the two selected scans. The corresponding linear fits and associated uncertainties are reported in Table B.1.

The complete set of scan timing plots for all other scan types used in electrical QC of

RD53B modules is provided in Appendix A.

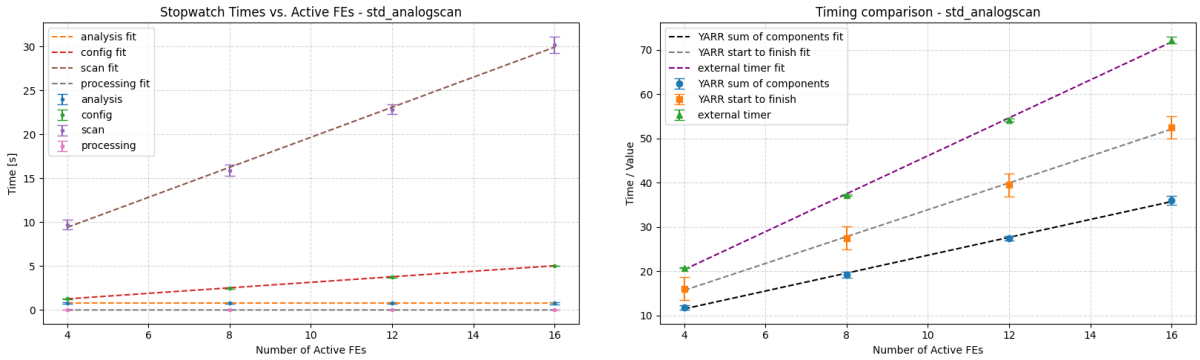

Figure 7.6.: Average duration of an analogue scan versus the number of active FEs. The left panel shows the breakdown by individual scan stages, while the right panel compares the total runtime measured using an external timer, the total time reported by the YARR framework, and the sum of the individual scan stages reported by YARR.

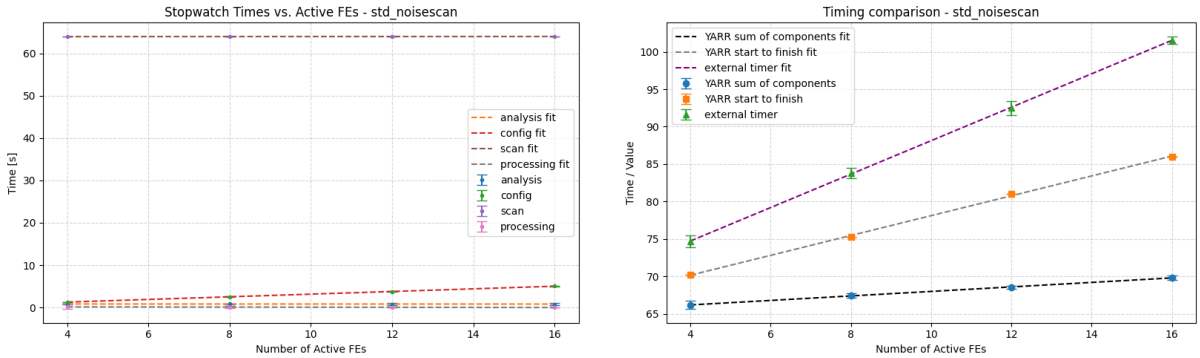

Figure 7.7.: Average duration of a noise scan versus the number of active FEs. The left panel shows the breakdown by individual scan stages, while the right panel compares the total runtime measured using an external timer, the total time reported by the YARR framework, and the sum of the individual scan stages reported by YARR.

The absolute time required to execute a scan for a given number of quad modules in parallel is summarised in Figure 7.8, providing a comprehensive overview of the scaling behaviour.

The calculated degree of parallelisation for each scan type and the number of quad modules (equivalently 4× the number of FEs) is visualised in Figure 7.9 with errors given through Gaussian error propagation with the standard deviation as previously used.

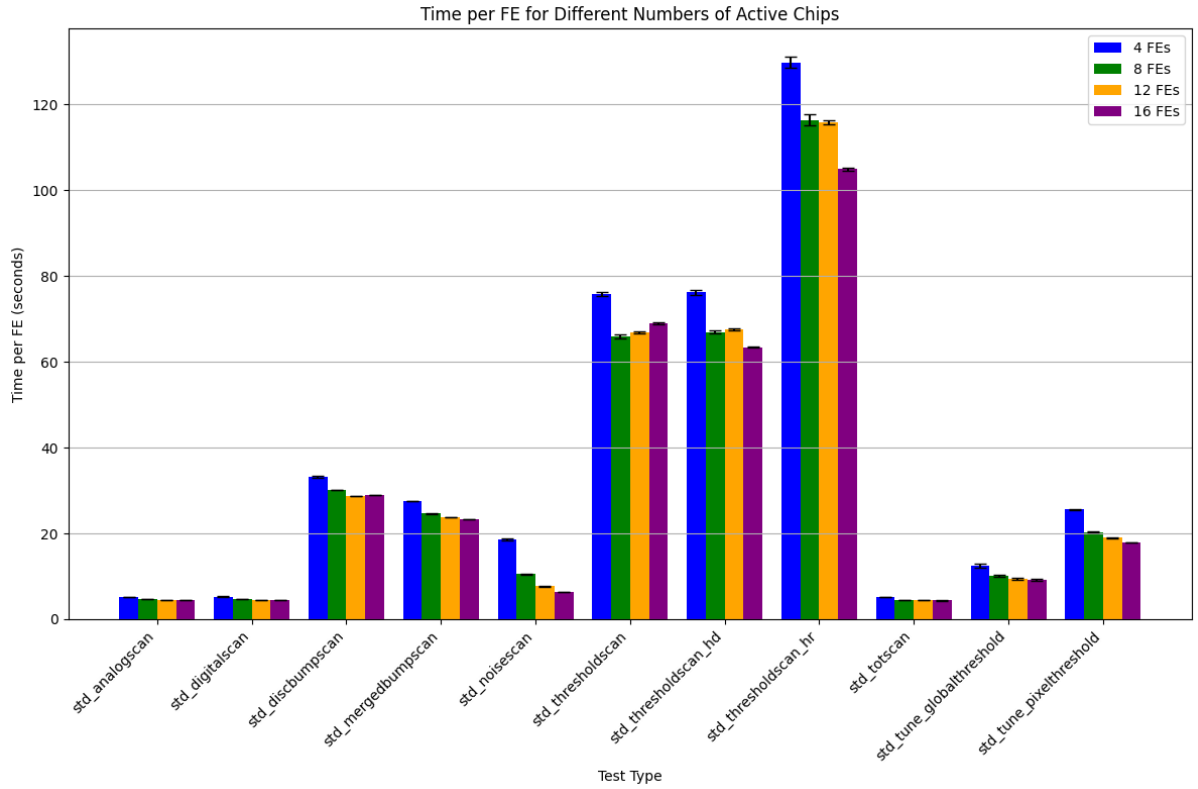

Figure 7.8.: Externally measured runtime for different scans in the QC routine across varying numbers of simultaneously operated quad modules.

7.2.4. Scan Routines

With the MHT, TUN, and PFA routines composed of the above-analysed scans as annotated in Figure 5.2, the total expected runtime of each routine for different numbers of quad modules can be determined. The resulting stacked bar plot, based on the results from before, is given in Figure 7.10.

Summarising this, the total parallelisation for a given number of modules, as well as the absolute time savings of a given configuration, can be calculated. The absolute time savings are given as the difference in total execution time when running the specified routine on n modules back to back one after another, as opposed to running the scans on all the modules simultaneously. The results are given in Table 7.2.

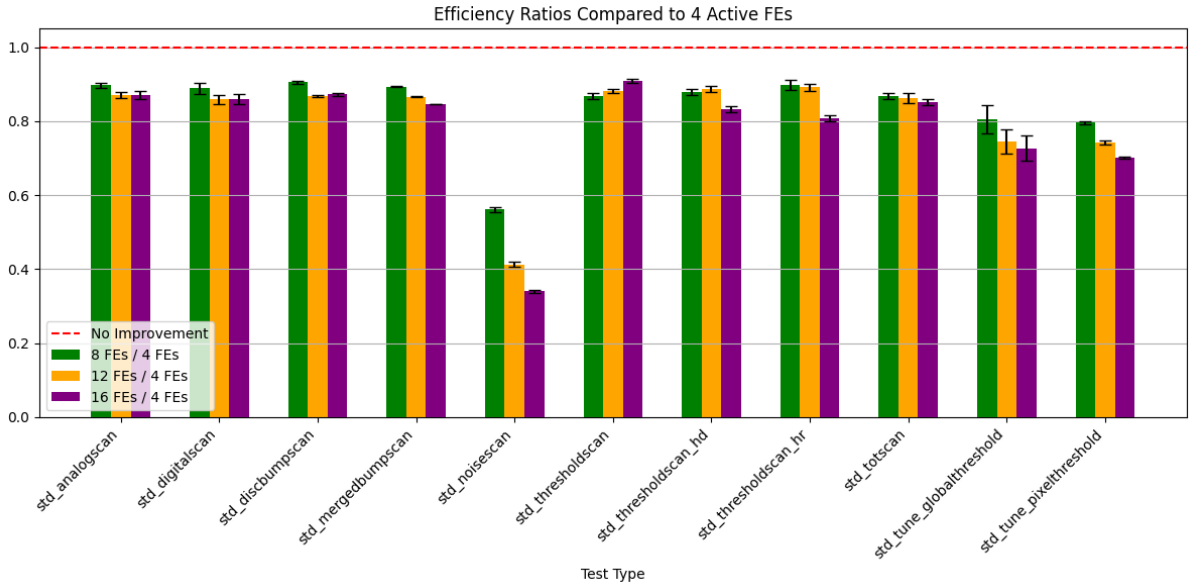

Figure 7.9.: Relative parallelisation efficiencies for different YARR scan types across varying numbers of active modules. Based on the externally measured runtime metric.

Routine	Modules	T. per mod. [s]	Par. eff. [%]	T. diff [m]
MHT	1	581 ± 6	-	-
	2	521 ± 6	89.6 ± 1.3	2.02 ± 0.27
	3	517 ± 3	88.9 ± 1.0	3.2 ± 0.4
	4	473.5 ± 1.8	81.4 ± 0.9	7.2 ± 0.5
TUN	1	1017 ± 11	-	-
	2	891 ± 9	87.6 ± 1.3	4.2 ± 0.5
	3	882 ± 5	86.7 ± 1.0	6.8 ± 0.6
	4	816 ± 4	80.3 ± 0.9	13.4 ± 0.8
PFA	1	663 ± 4	-	-
	2	561.4 ± 2.7	84.7 ± 0.7	3.38 ± 0.15
	3	544.6 ± 1.8	82.2 ± 0.6	5.90 ± 0.20
	4	546.5 ± 1.3	82.5 ± 0.5	7.75 ± 0.25

Table 7.2.: Summary of timing and parallel efficiency for routines PFA, MHT, and TUN. Listed are the Routine, the number of modules, the time per module, the parallelised efficiency as well as the time difference (time saved when running the specified number of modules simultaneously as opposed to sequentially).

It should be noted that the only YARR scan forming part of the current YARR-based

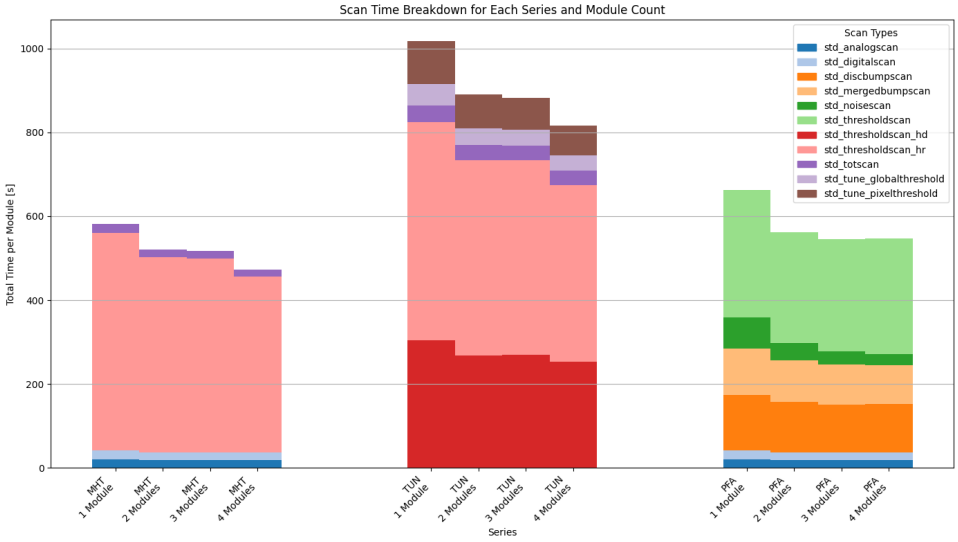

Figure 7.10.: Total scan time per module of the MHT, TUN, and PFA routines for different numbers of parallel running modules.

electrical QC routine, which could not be realistically tested within the scope of this thesis, is the source scan, executed after the cold electrical QC procedure, due to practical constraints when handling a radioactive source. A detailed analysis would have been complicated by the fact that there is only one Sr-90 source available, making it technically challenging to parallelise this particular scan.

8. Discussion

8.1. Electrical Characterisation

Due to errors encountered when running multiple modules, only the IV measurement could properly be analysed for parallelisability showing high parallelizability, while the remaining electrical characterisation tests could not be parallelised.

8.1.1. IV Measurement

The IV measurement demonstrates a high degree of parallelisability, as the results clearly show. This can be attributed to the use of individual high-voltage power supplies (HV PS) for each quad module. However, there is still room for improvement. Ideally, perfect parallelisation would result in a constant measurement time regardless of the number of modules under test.

# Modules	Minimum Parallelisation	Actual Parallelisation	Δp
2	50%	$(62.4 \pm 2.2)\%$	$(12.4 \pm 2.2)\%$
3	$33.\bar{3}\%$	$(49.2 \pm 2.2)\%$	$(15.9 \pm 2.2)\%$
4	25%	$(41.2 \pm 1.9)\%$	$(16.2 \pm 1.9)\%$

Table 8.1.: Comparison of ideal and achieved parallelisation for the IV measurements.

One reason for imperfect parallelisation is the blocking nature of the ramp-down phase of the power supplies. Although these phases are shorter than with alternative systems, they still impose a constant, unparallelisable component on the measurement process, preventing other processes from continuing during that time. Additionally, the GPIB interface used for communication may further limit parallelisation, as the current implementation (including the PC-side code) only allows one active communication at a time. As a result, HV PS devices may enter brief waiting cycles until the bus is available again.

8.1.2. Remaining Electrical Characterisation Tests

The remaining electrical characterisation tests did not demonstrate any parallelisability. Any attempt at simultaneous execution caused errors in all but one running instance.

The testing procedures as implemented in the `module-qc-tools` GitLab repository are not designed to handle more than one quad module simultaneously, as they all rely on YARR to execute the respective test. Since YARR itself cannot be parallelised across multiple instances, because each instance requires exclusive access to the FPGA card for communication with the connected modules, neither YARR nor, by extension, these remaining tests can be easily parallelised. Attempts to run these tests in separate threads or processes for two connected quad modules yielded consistent results: the first test would run successfully to completion, while any further concurrent test aborted after repeated failures to acquire the necessary lock for YARR instantiation. Although the `module-qc-tools` repository features both a `parallelisation` and a `multi-module` branch, these branches have remained stale for roughly a year, with continuously failing test builds and no active development. In a separate Merge Request [1], a partially functional multi-module ADC calibration was tested, achieving a runtime of approximately 15 minutes for a single quad module and a collective 53 minutes for four quad modules, corresponding to a parallelisation percentage of about 88 %. However, this implementation was never merged into the main codebase, making it impossible to reproduce these results on the current code base.

8.2. YARR Scans

The YARR scans for testing module functionality revealed a more complex parallelisation behaviour. In general, these scans can be executed in parallel when run in one singular instance, even benefiting from reduced execution times when running multiple modules simultaneously. However, the performance improvements vary between scan types. One key observation across all the scans carried out is the rather low deviation across repetitions of identical scans.

8.2.1. Version Comparison

The overall software functionality of YARR version 1.5.4 could be verified, as there were no significant differences across scans on the same modules between version changes. While this analysis is based on only a very limited number of scans-four scans per module and version, these results were deemed sufficient for continued operation during this thesis as

[1] See Merge Request #125 on GitLab.

the actual scan data was not of main interest here. Additionally, there is some degree of expected functionality associated with a release version of the critical QC software, implying that scans should execute properly.

8.2.2. Parallelizability

Scan Stages Analysing the durations of the individual scan stages (configuration, scan, processing, and analysis) recorded by YARR (see Figures A.1, left panels), a clear pattern emerges across all scan types. The processing and analysis stages contribute the least to the total runtime (around 1 s) and show nearly constant execution times, independent of the number of enabled front-end chips (FEs). In contrast, the configuration and scan stages exhibit linear time complexity depending on the number of active FEs. This behaviour is further quantified in the fit parameters visualised in Figure 8.1 and summarised in Table B.1.

For the configuration and processing stages, a clear clustering of fit parameters can be observed regardless of scan type, indicating consistent behaviour. Similarly, the analysis stage clusters around a central mean, with the exception of the HD threshold scan. As shown in Figure 8.1, both the processing and analysis stages have slopes near zero, indicating constant execution time and thus perfect parallelisability.

The configuration stage, while showing a consistent intercept across scan types, has a positive non-zero slope, implying linear runtime growth with an average slope of approximately 0.312 s per additional FE.

The scan stage shows considerable variation between scan types, which is expected, as the scan phase represents the primary functional difference between them.

In summary, the processing and analysis stages are perfectly parallelisable with constant runtime complexity, whereas the configuration stage exhibits linear complexity. The scan stages vary between scan types and should be considered linear individually.

Total Execution Time Overall, the total execution time based on external monitoring is consistently longer than the YARR-reported total runtime, which itself is consistently longer than the sum of the individual scan stage components.

Similar to the analysis above, the differences in slope and intercept values (including uncertainties) can be visualised by comparing pairs of the three measurement series. A weighted mean and standard deviation can then be calculated, as shown in Figure 8.2.

The differences in intercept values are minimal, hovering around zero across all pairs. This consistency suggests a negligible constant-time overhead. This implies that processes such as the spawning of an execution thread (as measured within the external timing as opposed to the YARR selfreported total time) has a negligable overhead and does not

significantly influence the runtime. Examining the slope differences reveals clustering around central mean values, indicating linear time-dependent differences between the individual measurement approaches. Part of this can be explained by overhead from additional command output before and after scans, the number of configuration files to be processed, and other FE-dependent processes.

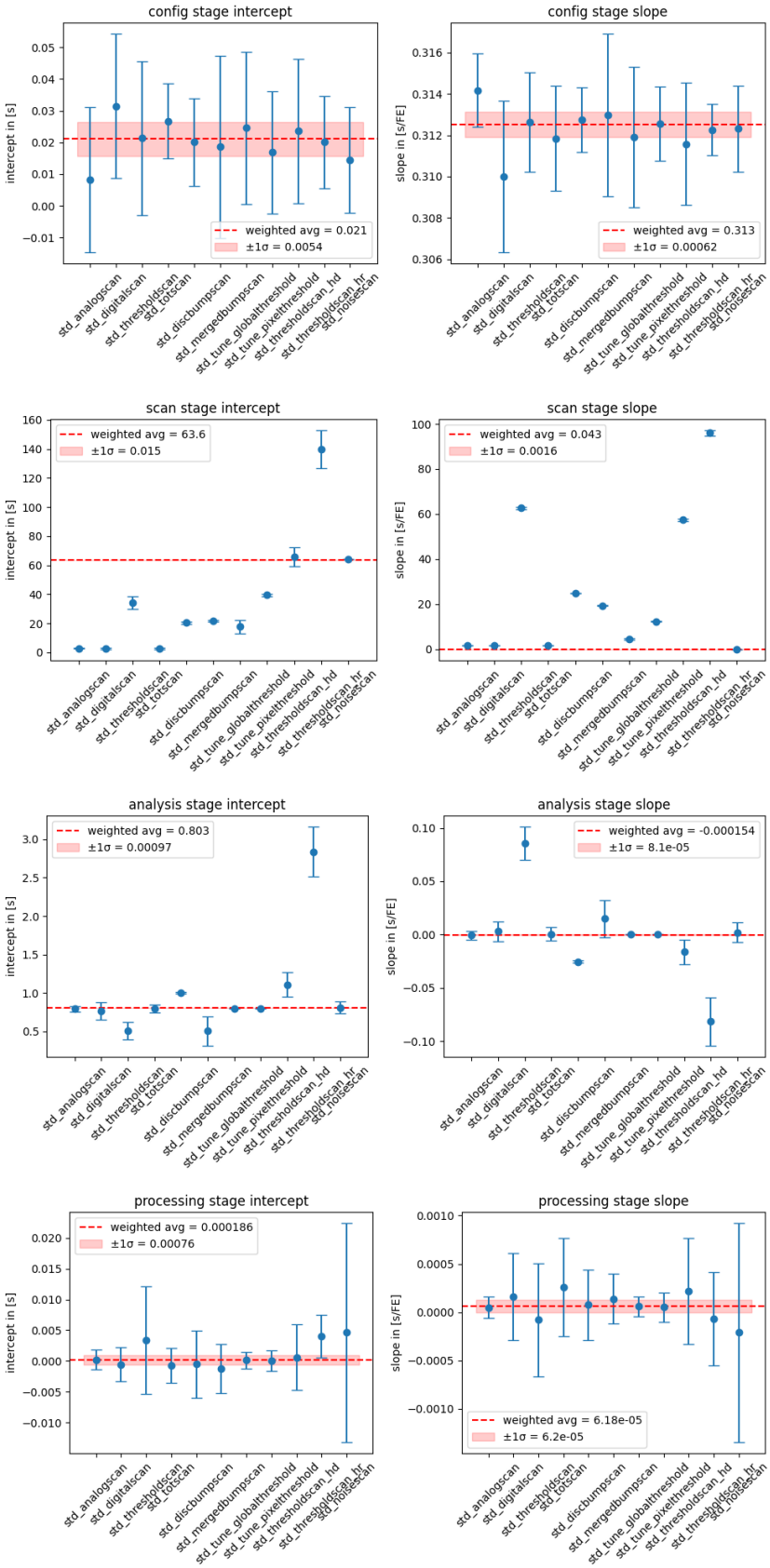

Figure 8.1.: Comparison of the optimised fit parameters (intercept b on the left and slope a on the right) for the configuration, scan, analysis, and processing stages across all scan types.

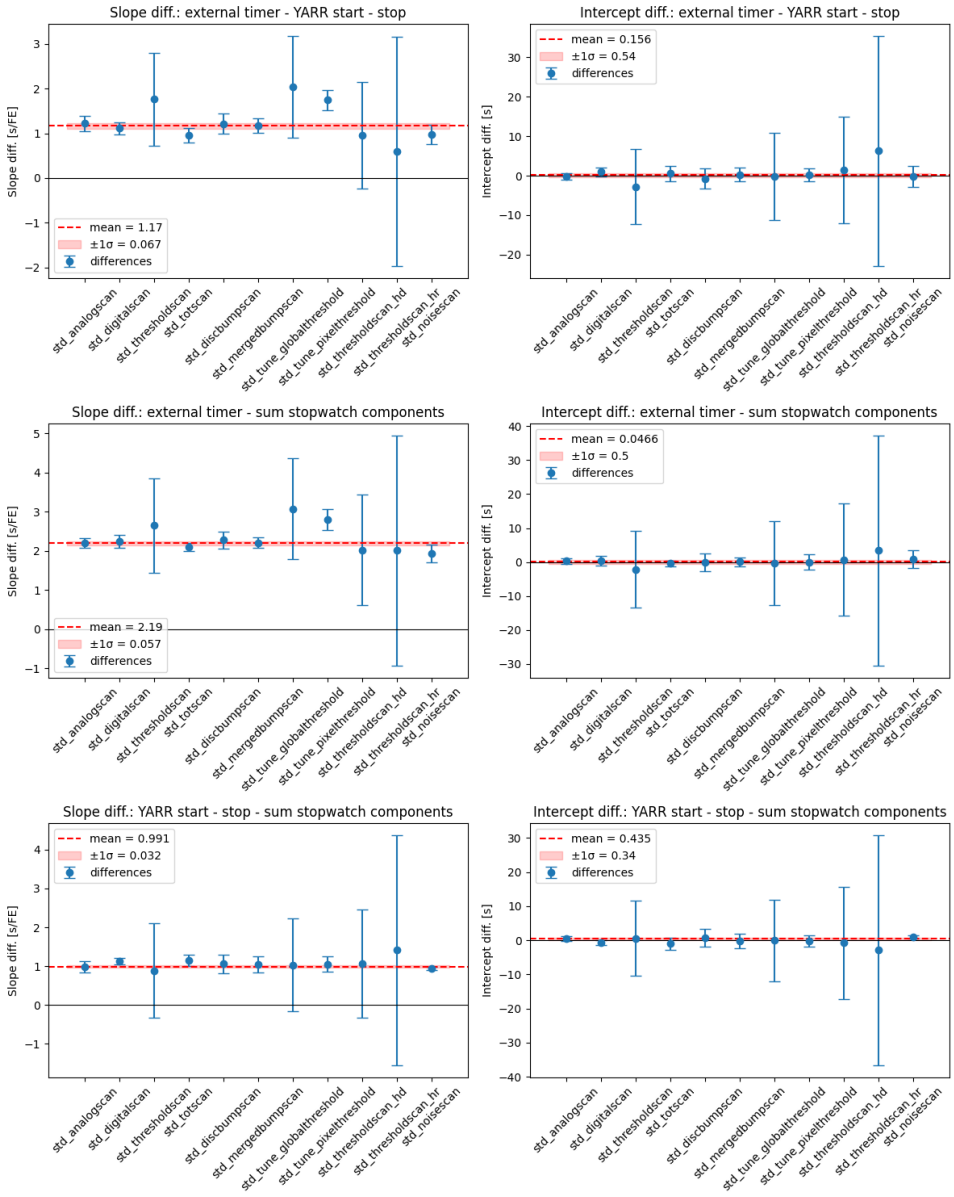

Figure 8.2.: Comparison of the fit parameters (intercept b on the left and slope a on the right) for the three duration measurement approaches using an external timer, the YARR inbuilt timer for start and finish time, as well as the sum of the YARR inbuilt stopwatch components.

9. Conclusion

This thesis has systematically explored the feasibility and performance of parallelising electrical quality control (QC) tests for silicon-based RD53B quad modules using the YARR software framework. Motivated by the expected ramp-up of module production, the work aimed to optimise QC throughput while preserving procedural reliability.

The analysis shows that IV measurements can be parallelised effectively, primarily due to the use of separate high-voltage power supplies per module. This allowed for substantial time savings, such as a runtime reduction from 58 minutes to 49 minutes when running four modules simultaneously.

However, other electrical characterisation tests-such as tuning and noise scans-face considerable limitations. The current software tools, particularly `module-qc-tools` and YARR, do not support multiple concurrent instances, as each requires exclusive access to the FPGA. Attempts at parallel execution failed due to resource conflicts, and experimental branches designed for multi-module support have seen no recent development.

Even sensor functionality tests (MHT, TUN, PFA), which showed some benefit from parallel execution, are constrained by synchronisation requirements: modules must wait for others to complete earlier stages in order to benefit from multiprocessing, reducing the overall gain.

Given these software limitations and the rigid serial powering hardware, full parallelisation across all tests is currently impractical. A major codebase overhaul of the *module-qc-tools* would be required, unlikely to occur before the imminent start of the production phase, where testing procedures must remain stable.

Nonetheless, some improvements remain possible. A more flexible powering setup allowing for dynamic use of one to four modules would improve adaptability. Moreover, the non-electrical, labour-intensive parts of the workflow deserve further analysis, as they could present significant opportunities for increasing throughput.

In summary, while selective parallelisation, especially of IV measurements, is both feasible and beneficial, a broader implementation across all tests will require coordinated software and hardware upgrades. Strategic improvements in these areas could significantly enhance the efficiency and scalability of the QC process.

10. Outlook

With the release of YARR v1.5.5, it would be valuable to reassess test performance and runtime behaviour under the new version. It may offer improved stability or parallelisability not available in earlier versions. In addition, a comparative study using production-grade ITkPixV2 sensors is recommended, as they may exhibit different scan durations or require slight modifications to the QC procedure and scan types. To further optimise the QC workflow, a detailed analytical or simulation-based model should be developed. This model should account for resource limitations, module availability, and yield rates to better schedule and balance tests across available infrastructure and personnel. Understanding the causes of observed timing variations between different timing measurements will require improved runtime monitoring and possibly deeper inspection of the YARR software.

To streamline the QC workflow, a dedicated simulation tool could be developed to optimize module handling and resource allocation. Such a tool should account for execution time, test sequencing, and the availability of both human and technical resources.

Finally, with the climate chamber now fully configured to perform all essential electrical tests, except the radioactive source scan, it can (and to some degree already is) be incorporated into the overall QC process. Doing so could help mitigate bottlenecks and improve overall throughput during the production phase.

A. Scan durations

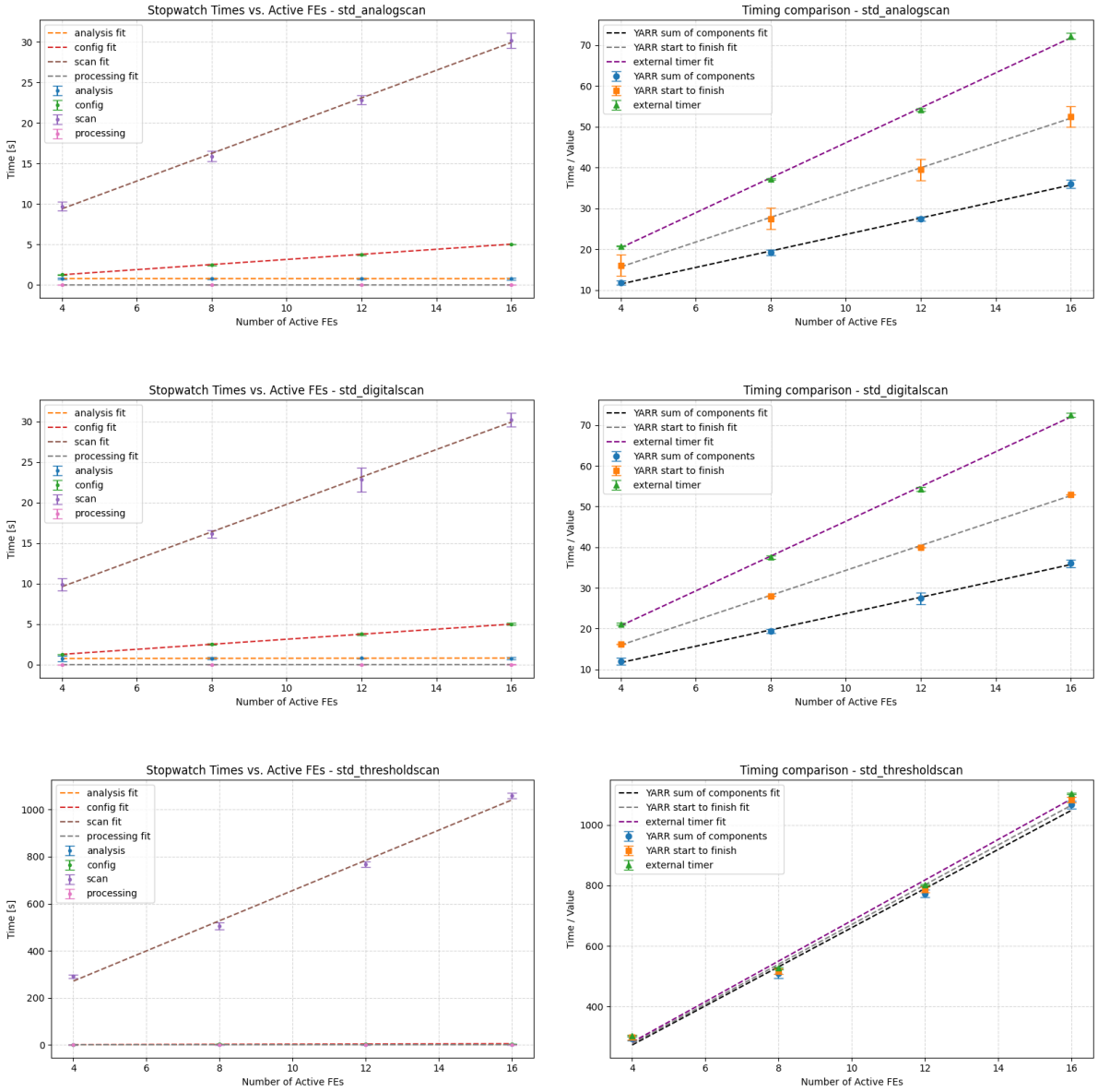

Figure A.1.: Timing performance of scans used in RD53B electrical QC (part 1).

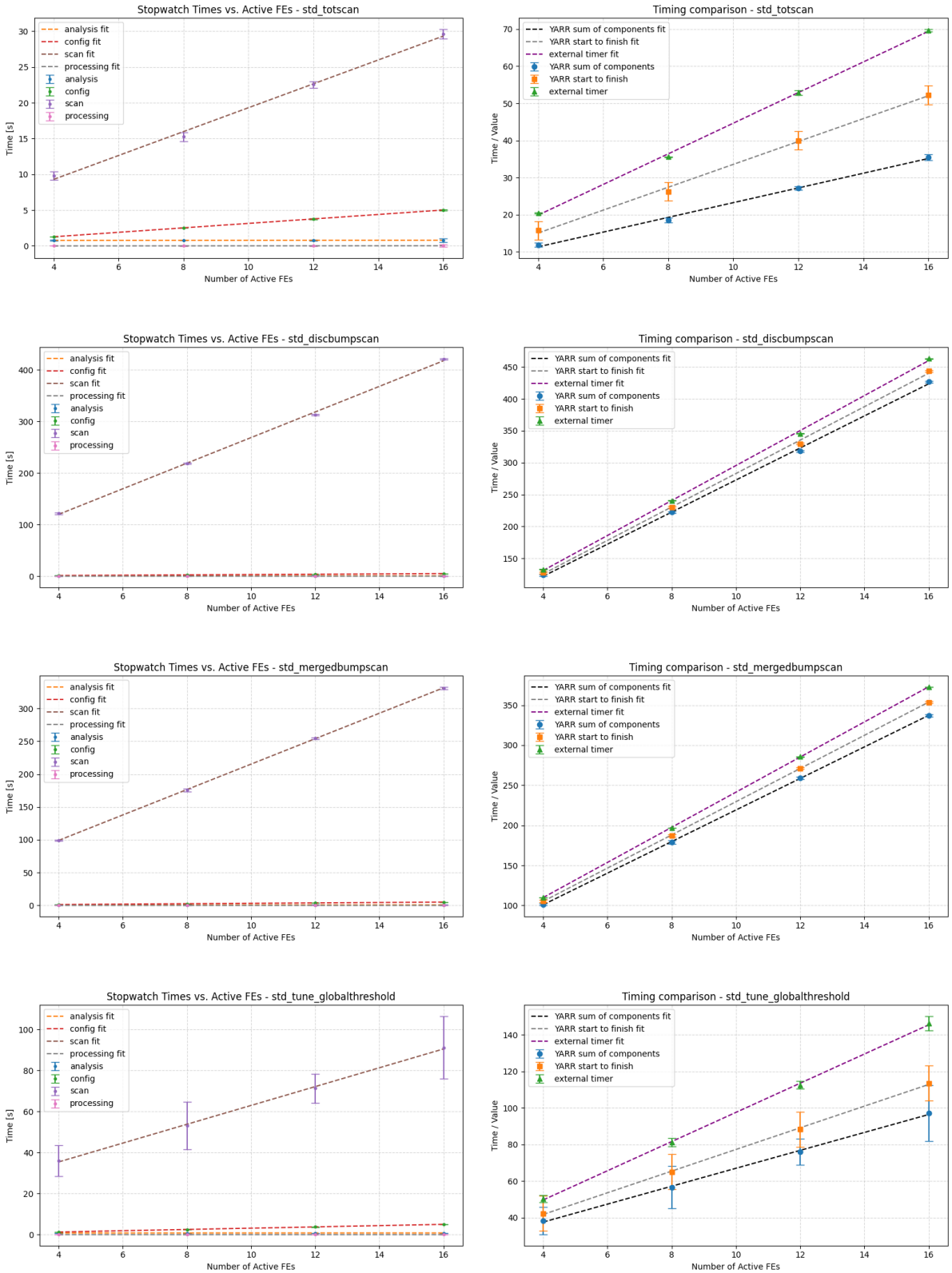

Figure A.1.: Timing performance of scans used in RD53B electrical QC (part 2).

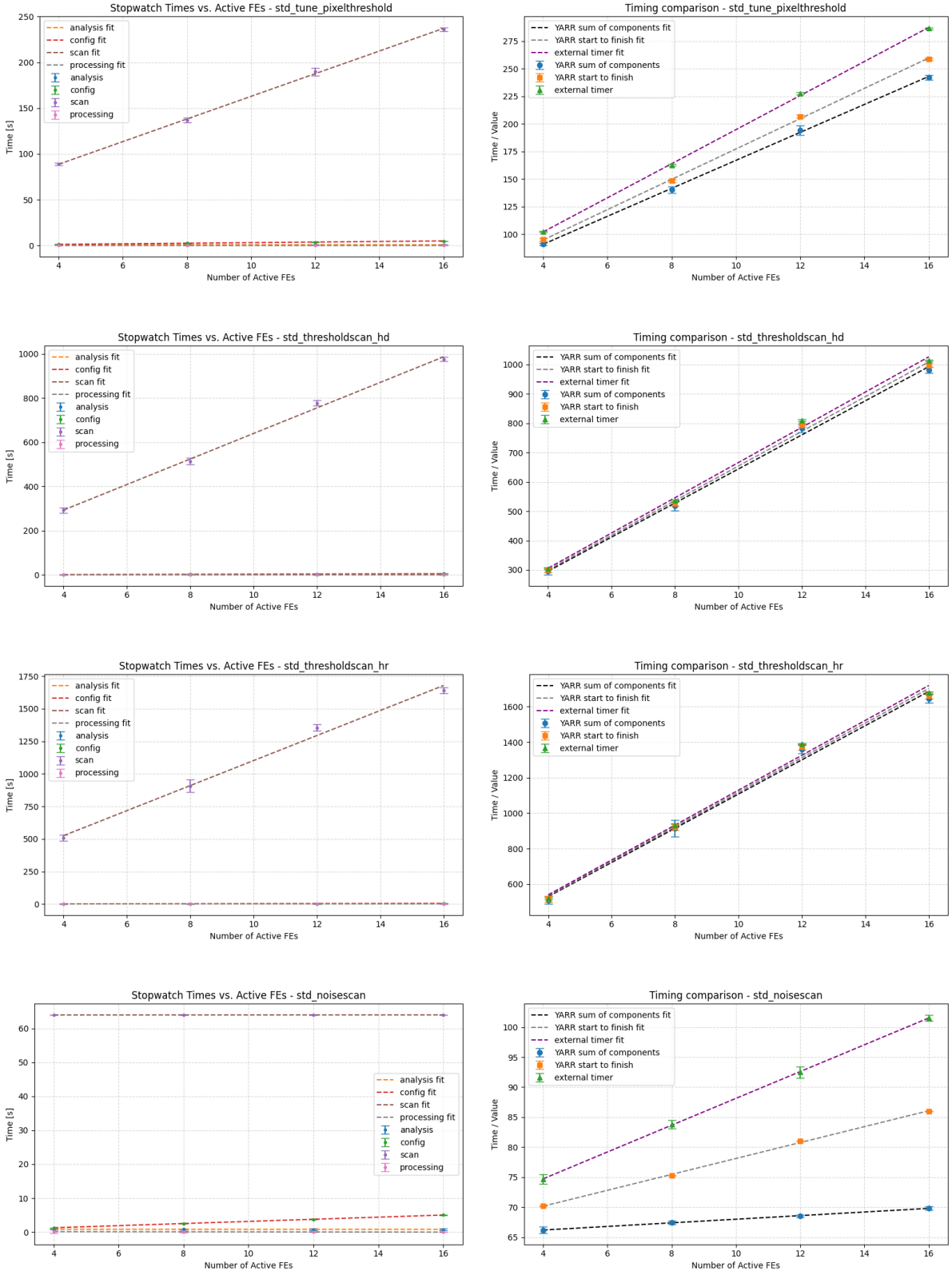

Figure A.1.: Timing performance of all scan types used in RD53B electrical QC as a function of the number of active FEs. Each pair shows: (left) breakdown of the scan duration by stage, and (right) comparison of external total runtime, YARR self-reported runtime, and summed YARR scan stage durations. The corresponding fit function parameters are summarised in table B.1 and B.2.

B. Fit Functions

Scantype	stage	Intercept [s]	Slope [s/FE]	χ^2_{red}
analogscan	external timer	3.9 ± 0.7	4.19 ± 0.11	0.23
	YARR start - stop	4.1 ± 0.6	2.97 ± 0.14	0.10
	sum o. components	3.6 ± 0.7	1.99 ± 0.07	0.55
digitalscan	external timer	3.9 ± 1.2	4.24 ± 0.14	0.22
	YARR start - stop	3.000 ± 0.009	3.1250 ± 0.0009	0.20
	sum o. components	3.7 ± 0.8	1.99 ± 0.09	0.32
thresholdscan	external timer	33 ± 8	65.8 ± 0.8	11.92
	YARR start - stop	35 ± 7	64.0 ± 0.8	12.62
	sum o. components	35 ± 9	63.1 ± 1.0	6.84
totscan	external timer	3.2 ± 0.8	4.06 ± 0.10	3.14
	YARR start - stop	2.7 ± 1.8	3.11 ± 0.15	0.63
	sum o. components	3.7 ± 0.6	1.96 ± 0.06	1.74
discbumpscan	external timer	19.9 ± 1.8	27.54 ± 0.15	12.39
	YARR start - stop	20.6 ± 1.9	26.33 ± 0.17	6.26
	sum o. components	19.9 ± 2.0	25.27 ± 0.17	10.21
mergedbumpscan	external timer	22.5 ± 0.5	21.89 ± 0.05	0.58
	YARR start - stop	22.14 ± 1.8	20.73 ± 0.16	0.23
	sum o. components	22.41 ± 1.3	19.68 ± 0.13	0.21
tune globalthreshold	external timer	18 ± 9	7.9 ± 0.9	0.02
	YARR start - stop	19 ± 8	5.8 ± 0.8	0.02
	sum o. components	19 ± 9	4.8 ± 1.0	0.01
tune pixelthreshold	external timer	40.5 ± 1.6	15.40 ± 0.21	0.34
	YARR start - stop	40.37 ± 0.5	13.66 ± 0.11	0.44
	sum o. components	40.5 ± 1.7	12.61 ± 0.18	0.36
thresholdscan hd	external timer	68 ± 10	59.7 ± 0.9	4.90
	YARR start - stop	67 ± 10	58.7 ± 0.9	4.65
	sum o. components	66.8 ± 13.4	57.7 ± 1.2	2.86

Table B.1.: Summary of linear fit parameters (part 1) for different timing methods used in Figures A.1. Continued on next page.

Scantype	stage	Intercept [s]	Slope [s/FE]	χ^2_{red}
thresholdscan hr	external timer	146 ± 21	98.2 ± 1.8	11.47
	YARR start - stop	140 ± 21	97.6 ± 1.9	9.65
	sum o. components	143 ± 27	96.2 ± 2.4	6.00
noisescan	external timer	65.8 ± 2.7	2.23 ± 0.22	0.00
	YARR start - stop	66.0 ± 0.05	1.251 ± 0.004	0.33
	sum o. components	65.0 ± 0.5	0.30 ± 0.04	0.03

Table B.2.: Summary of linear fit parameters (part 2) for different timing methods used in Figures A.1.

Scantype	stage	Intercept [s]	Slope [s/FE]	χ^2_{red}
analogscan	analysis	$.79 \pm .04$	$-0.001 \pm .005$	0.03
	config	$.008 \pm .023$	$.3142 \pm .0018$	0.06
	scan	$2.8 \pm .4$	$1.68 \pm .04$	2.09
	processing	$.0002 \pm .0017$	$4.84078 \pm .00012$	0.00
digitalscan	analysis	$.76 \pm .12$	$.003 \pm .0010$	0.10
	config	$.031 \pm .023$	$.310 \pm .004$	0.03
	scan	$2.7 \pm .4$	$1.70 \pm .05$	1.46
	processing	$-0.0005 \pm .0028$	$.0002 \pm .0005$	0.08
thresholdscan	analysis	$.51 \pm .12$	$.086 \pm .016$	0.07
	config	$.021 \pm .025$	$.3126 \pm .0024$	0.41
	scan	34 ± 5	$62.7 \pm .5$	26.88
	processing	$.003 \pm .009$	$-7.9839 \pm .0006$	0.05
totscan	analysis	$.79 \pm .06$	$.000 \pm .007$	0.52
	config	$.027 \pm .012$	$.3118 \pm .0026$	0.01
	scan	$2.7 \pm .4$	$1.657 \pm .0210$	6.73
	processing	$-0.0008 \pm .0029$	$.0003 \pm .0006$	0.06
discbumpscan	analysis	$1.006 \pm .009$	$-0.0254 \pm .00010$	0.31
	config	$.020 \pm .014$	$.3128 \pm .0016$	0.12
	scan	$20.5 \pm .9$	$24.710 \pm .08$	59.34
	processing	$-0.001 \pm .006$	$7.6932 \pm .0004$	0.00

Table B.3.: Summary of linear fit parameters (part 1) for each scantype, as visualised in 8.1. Continued on next page.

Scantype	stage	Intercept [s]	Slope [s/FE]	χ^2_{red}
mergedbumpscan	analysis	$.50 \pm .19$	$.015 \pm .018$	0.46
	config	$.019 \pm .029$	$.313 \pm .004$	0.02
	scan	$21.8 \pm .7$	$19.36 \pm .07$	0.58
	processing	$-0.001 \pm .004$	$.00014 \pm .00026$	0.02
tune globalthreshold	analysis	$.8003 \pm .0022$	$.00015 \pm .000110$	0.06
	config	$.025 \pm .025$	$.312 \pm .004$	0.06
	scan	18 ± 5	$4.5 \pm .5$	0.04
	processing	$.0001 \pm .0014$	$5.86043 \pm .00011$	0.10
tune pixelthreshold	analysis	$.8007 \pm .0011$	2 ± 9	0.11
	config	$.017 \pm .0110$	$.3126 \pm .0018$	0.10
	scan	$39.7 \pm .8$	$12.29 \pm .09$	1.47
	processing	$-1.8242 \pm .0017$	$4.999910 \pm .00016$	0.01
thresholdscan hd	analysis	$1.11 \pm .17$	$-0.016 \pm .012$	3.28
	config	$.024 \pm .023$	$.3116 \pm .00210$	0.05
	scan	66 ± 7	$57.4 \pm .6$	11.68
	processing	$.001 \pm .006$	$.0002 \pm .0006$	0.03
thresholdscan hr	analysis	$2.8 \pm .4$	$-0.082 \pm .023$	25.91
	config	$.020 \pm .015$	$.3123 \pm .0013$	0.44
	scan	1310 ± 14	96.0 ± 1.2	23.53
	processing	$.004 \pm .004$	$-7.1964 \pm .0005$	0.05
noisescan	analysis	$.81 \pm .08$	$.002 \pm .0010$	0.40
	config	$.014 \pm .017$	$.3123 \pm .0021$	0.25
	scan	$63.9910 \pm .016$	$.0017 \pm .0017$	0.01
	processing	$.005 \pm .018$	$-0.0002 \pm .0012$	0.34

Table B.4.: Summary of linear fit parameters (part 2) for each scantype, as visualised in 8.1.

Bibliography

[1] I. Zurbano Fernandez, et al., *High-Luminosity Large Hadron Collider (HL-LHC): Technical design report* **10/2020** (2020)

[2] *Technical Design Report for the ATLAS Inner Tracker Pixel Detector* (2017)

[3] D. Müller, *German Cluster Report 2025-06-26: (Pre-)Production Status Report*, Internal Report (2025), on behalf of the German Cluster: Uni Bonn, Uni Göttingen, Uni Siegen, and MPP Munich

[4] M. Thomson, *Modern particle physics*, Cambridge University Press, New York (2013)

[5] Cush, *Standard Model of Elementary Particles* (2019), URL `https://en.wikipedia.org/wiki/File:Standard_Model_of_Elementary_Particles.svg`

[6] S. Weinberg, *A Model of Leptons*, Phys. Rev. Lett. **19**, 1264 (1967)

[7] H. Fritzsch, M. Gell-Mann, H. Leutwyler, *Advantages of the Color Octet Gluon Picture*, Phys. Lett. B **47**, 365 (1973)

[8] P. Skands, *Introduction to QCD*, in *Searching for New Physics at Small and Large Scales*, WORLD SCIENTIFIC (2013)

[9] G. Altarelli, *A QCD primer*, AIP Conf. Proc. **631(1)**, 70 (2002)

[10] G. Aad, et al. (ATLAS), *Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC*, Phys. Lett. B **716**, 1 (2012)

[11] S. Chatrchyan, et al. (CMS), *Observation of a New Boson at a Mass of 125 GeV with the CMS Experiment at the LHC*, Phys. Lett. B **716**, 30 (2012)

[12] S. Navas, et al. (Particle Data Group), *Review of particle physics*, Phys. Rev. D **110(3)**, 030001 (2024)

[13] L. Evans, *The Large Hadron Collider (LHC)*, New J. Phys. **9**, 335 (2007)

[14] *LHC Design Report Vol.1: The LHC Main Ring* (2004)

[15] *ATLAS Technical Proposal for a General-Purpose pp Experiment at the Large Hadron Collider at CERN*, CERN/LHCC/94-43, LHCC/P2, 1994 (unpublished)

[16] S. Mehlhase (ATLAS Collaboration), *ATLAS detector slice (and particle visualisations)* (2021), URL `https://cds.cern.ch/record/2770815`

[17] *ATLAS magnet system: Technical design report* (1997)

[18] D. Dominguez, K. P. Moles, S. Mehlhase (ATLAS), *ATLAS detector schematics* (2021), URL `https://cds.cern.ch/record/2777214`

[19] H. Bethe, *Theory of the Passage of Fast Corpuscular Rays Through Matter*, Annalen Phys. **5**, 325 (1930)

[20] H. A. Bethe, *Nuclear Dynamics*, Rev. Mod. Phys. **9(2)**, 69 (1937)

[21] H. Kolanoski, N. Wermes, *Particle Detectors*, Oxford University Press (2020)

[22] C. Grupen, I. Buvat, editors, *Handbook of Particle Detection and Imaging*, Springer, Berlin, Germany (2012)

[23] G. Aad, et al., *ATLAS pixel detector electronics and sensors*, JINST **3**, P07007 (2008)

[24] L. Rossi, et al., *Pixel Detectors. From Fundamentals to Applications*, Particle Acceleration and Detection, Springer (2006)

[25] C. W. Fabjan, F. Gianotti, *Calorimetry for particle physics*, Rev. Mod. Phys. **75**, 1243 (2003)

[26] W. Shockley, *Currents to conductors induced by a moving point charge*, J. Appl. Phys. **9(10)**, 635 (1938)

[27] S. Ramo, *Currents induced by electron motion*, Proc. Ire. **27**, 584 (1939)

[28] ATLAS Collaboration, *ITk Pixel Layout Updates*, ATLAS Technical Report ITK-2020-002, CERN (2020), ATLAS plots ITK-2020-002

[29] H. Pernegger (ATLAS Collaboration), *Overview of the ATLAS ITk Pixel detector project* (2023), ATL-INDET-SLIDE-2023-265, CDS 2878575

[30] A. Sharma (ATLAS Collaboration), *Module development for the ATLAS ITk Pixel Detector*, Technical report, CERN, Geneva (2024), CDS 2889411

[31] M. Saimpert (ATLAS Collaboration), *Module development for the ATLAS ITk Pixel Detector*, Technical report, CERN, Geneva (2024), CDS 2896648

[32] *RD53B Users Guide*, Technical report, CERN, Geneva (2020), CDS 2754251

[33] F. Munoz Sanchez (ATLAS ITk pixel), *Carbon Based Local Supports for the ATLAS ITk Pixel Detector*, PoS **Pixel2022**, 077 (2023)

[34] F. J. M. Sanchez, the ATLAS Collaboration, *ATLAS ITk Pixel Detector Overview*, in *Proceedings of the 42nd International Conference on High Energy Physics (ICHEP 2024)*, page 878, Prague, Czech Republic (2025), ATL-ITK-PROC-2024-038

[35] M. Marjanović, et al., *Electrical Specification and Quality Control Procedures for ITkPixV1.1 Modules*, Technical Report AT2-IP-QA-0025, ATLAS Collaboration (2024), revision 388096b1, available on GitLab

[36] N. Grün, *Quality Control of ITk Modules at the University of Göttingen*, Master's thesis, University of Göttingen (2023), II.Physik-UniGö-BSc-2023/09

[37] Y. Tian, *Final Steps Towards Production of the ITk Pixel Detector for the ATLAS High Luminosity Upgrade*, Ph.D. thesis, University of G (2024), II.Physik-UniGö-Diss-2024/02

[38] R. Förster, Private communication with the author on 02 Oct 2025

Acknowledgements

I would like to express my heartfelt gratitude to all those who have supported me throughout this journey.

First and foremost, I extend my sincerest thanks to Prof. Arnulf Quadt for providing me with the opportunity to work on such a fascinating and relevant topic in ITk development. I am also deeply grateful to apl. Prof. Dr. Jörn Große-Knetter for his excellent and hands-on help. Your expertise and willingness to assist have greatly enhanced my learning experience. I would also like to thank PD. Dr. Markus Keil for being the second examiner.

A special thanks to Ruben Förster for his continued support, both in the lab and outside of it. No matter the place or time, I could always count on you to answer any and all of my questions. Your positive attitude and our engaging conversations have made this journey all the more enjoyable. Additionally, I want to thank the entire working group for their warm welcome and collaborative spirit. It has been a pleasure working alongside you.

Last but not least, I would like to express my deepest gratitude towards my parents, siblings, and girlfriend for their everlasting support.

Erklärung nach §13(9) der Prüfungsordnung für den Bachelor-Studiengang Physik und den Master-Studiengang Physik an der Universität Göttingen:
Hiermit erkläre ich, dass ich diese Abschlussarbeit selbständig verfasst habe, keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe und alle Stellen, die wörtlich oder sinngemäß aus veröffentlichten Schriften entnommen wurden, als solche kenntlich gemacht habe.
Darüberhinaus erkläre ich, dass diese Abschlussarbeit nicht, auch nicht auszugsweise, im Rahmen einer nichtbestandenen Prüfung an dieser oder einer anderen Hochschule eingereicht wurde.

Göttingen, den 9. Oktober 2025

(Leander Teich)